

# A Study on the Design Aspects of Interleaved Boost Converter for Telecommunication Systems

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**Abstract**— This paper highlights the importance of interleaved boost converter for Telecommunication Systems. The design aspects of interleaved boost converter with zero-voltage switching (ZVS) and zero-current switching (ZCS) is discussed in detail. The study includes the description of switch mode power supply, DC-DC Converter along with the characteristics of power MOSFET switches and soft switching principle. The selection of inductor, output capacitor, and freewheeling diodes, and main switches, number of phases and choice of duty ratio for the proposed IBC in telecom sector is investigated. Theoretical analysis is carried out to emphasize the significance of IBC as a suitable power converter for telecommunication systems.

**Index Terms**— Interleaved boost converter, DC-DC Converter, soft switching, zero-voltage switching (ZVS), zero-current switching (ZCS)

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## I. INTRODUCTION

In the present scenario, the power system equipments of telecom sector require power converters operating with high efficiency and power-density. The design of power converter basically depends on the choice of power semiconductor devices. It has therefore become essential to study about power MOSFET switching characteristics which has to be operated at high switching frequencies to cancel the output ripple voltages.

Various power converter topologies is discussed in the literature but the best approach is the interleaving technique [1]-[3] which gives a high power-density and the benefits of increased switching frequencies without compromising the efficiency. Generally, interleaving offers a size reduction of magnetic components and other performance benefits by processing power in a number of power conversion stages that are connected in parallel. By phase shifting (interleaving)of the switching instances of the parallel modules, the obvious switching frequency of the converter increases as several times as the number of the interleaved modules. Besides the size reduction of magnetic components, the interleaving technique offers reduced input current and output-filter capacitor current due to a ripple cancellation effect.

Converters with interleaved operation are fascinating techniques nowadays. Interleaved boost converters are applied as power-factor-correction front ends [3]–[5]. Several soft-switching techniques, gaining the features of zero-voltage switching (ZVS) or zero-current switching (ZCS) for dc/dc converters [4]–[7], have been proposed to substantially reduce the switching losses, and hence, attain high efficiency at higher switching frequencies. There are many resonant or quasi-resonant converters with the advantages of ZVS or ZCS presented earlier [8]. The main problem with these kinds of converters is that the voltage stresses on the power switches are too high in the resonant converters, especially for the high-input dc-voltage applications. Passive snubbers achieving ZVS are attractive [9 - 12], since no extra active switches are needed, and therefore, feature a simpler control scheme and lower cost. In this paper, ZVS/ZCS based IBC is investigated for telecom sector. A detailed theoretical study [13 - 14], is carried out in this paper to exploit the benefits of interleaving principle in DC-DC converters and a simple guidance is provided in designing the proposed IBC for communication systems.

## II. SWITCH MODE POWER SUPPLY

DC voltage power supplies are utilized in most electrical/electronic equipment in order to meet the power requirement of the electronic circuits. The power range of an SMPS can be from several watts, up to hundreds of kilowatts. Typical applications of an SMPS include computer power supplies, house appliance power supplies, battery chargers, telecommunication power supplies, welding machines, DC motor drives, etc. The basic block diagram of an SMPS system is depicted in Figure 1.

The unregulated input voltage is supplied from the AC supply; typically, the AC line voltage that is either single-phase or three-phase is rectified to DC voltage by a diode bridge rectifier. The diode bridge output voltage is filtered by a large electrolytic capacitor so that ripple voltage magnitude of the unregulated DC voltage is reduced. The heart of an SMPS system is formed by a switch mode DC/DC converter that outputs the regulated DC voltage.

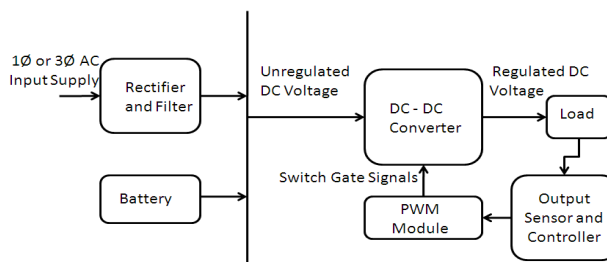


Fig. 1 Block Diagram of Switch Mode Power Supply

### III. DC – DC CONVERTER

A DC – DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically the output produced is at a different voltage level than the input. The DC – DC converter block mainly utilizes power semiconductor devices (switches), passive filter components, and an isolation transformer when galvanic isolation is necessary. The power semiconductor devices may be either gate controlled switching devices including Bipolar Junction Transistors (BJTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) or uncontrolled (naturally commutated) devices which are power diodes. The passive components are utilized either for AC voltage and current conversion with isolation (transformers) or for energy storage (inductors and capacitors). The output sensor and controller block consists of measurement and control circuits. For power supply design, mostly MOSFETs are widely used as switching devices. It is essential that MOSFETs designed for high-efficiency, high-switching-frequency applications (> 300 kHz) have a few key attributes for meeting the ever increasing demand for high power densities with high converter efficiency. The key attributes are:

1. Very low on-resistance is essential for minimizing synchronous rectifier and controlling MOSFET conduction losses. Low drain to gate resistance  $R_{DS}$  (ON) in a discrete MOSFET implies that the package and the silicon resistive contributions are very low.
2. Low internal series gate resistance ( $R_G$  or gate ESR) is important. A discrete power MOSFET is often depicted (or modeled) as a lumped circuit consisting of parasitic capacitance and resistance of the active cell scaled for area, where the MOSFET internal gate resistance and internal capacitance determine the input impedance and switching speeds.
3. Low parasitic package inductance, which is important for optimizing MOSFET switching speed and is required for minimizing the voltage stresses associated with  $L \times di/dt$  during switching transitions.
4. Low thermal resistance (junction-to-case and junction-to-ambient) for removal of self-generated heat from the MOSFET silicon and package increases reliability and provides for minimized power losses with higher system efficiencies.
5. Robust Forward Biased Safe Operating Area (FBSOA) and Unclamped Inductive Switching (UIS) are typically highly correlated and provide insurance for surviving high-energy switching spikes within the converter.

### IV. RESONANT SWITCHING

In DC/DC converter circuit, the switches are generally considered to operate in the hard-switching operating condition, which corresponds to the voltage and current simultaneously being large during switching and implies considerable switching loss and stress on the devices as shown in Fig. 2. Switching losses are a major limiting factor on the switching frequency. In order to maintain a high energy efficiency and acceptable cost in the converter, the switching frequency is confined to a practically acceptable range. The reduced switching frequency results in larger passive components (transformer, inductor and capacitor) and heavier DC/DC converters, which is a considerable drawback of the industrial equipment power supply.

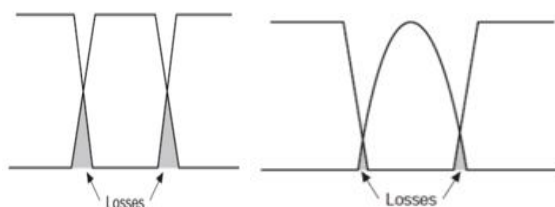


Fig. 2. Hard Switching

Fig. 3. Resonant Switching

Soft-switching techniques, when applicable to a power converter, aid in energy efficiency enhancement, increase in switching frequency (passive component size and weight reduction), switching device electrical/thermal stress reduction, EMI reduction, and cost reduction. In a soft-switching circuit, the switches commute at zero voltage or current. Soft-switching process is provided in the DC/DC converter circuit with a resonant switch, which consists of a controllable semiconductor switch (S), a reverse parallel external diode (freewheeling diode), and a resonant inductor ( $L_R$ ) or a resonant capacitor ( $C_R$ ).

### Zero Current Switching (ZCS) Operation

Soft-switching of the controllable switch can be provided using either Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) technique. For the resonant switch providing ZCS operation, a resonant inductor ( $L_R$ ) is connected in series with the controllable switch, as shown in Figure 4.a. When the switch is in off-state, the inductor current is zero; an opportunity exists for soft turn on. Since the inductor current is continuous and cannot change instantaneously, with sufficient  $L_R$  the device fully turns-on (the voltage across the switch ( $V_S$ ) is reduced to the on-state value) before the inductor current reaches a significant value. Hence, there exists only a small amount of switching power loss at turn-on process. The turn-off process for ZCS operation is accomplished by the resonance operation between  $L_R$  and an external capacitor which is not included in Figure 4a. The capacitor may be connected either in series with or parallel to the resonant switch based on the converter circuit topology. Once, the resonance transition begins the current decreases to zero. Thus, the opportunity for zero current turn-offs is created. As a result of this resonance,  $V_S$  starts to increase after  $I_S$  reduced to zero, hence ZCS is satisfied during turn-off switching interval also.

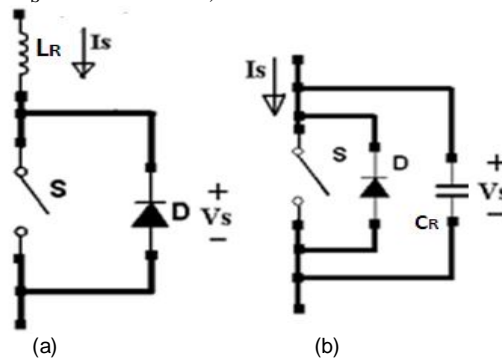


Fig. 4. The Elementary Resonant Switches for: (a) ZCS, and (b) ZVS Operation.

### Zero Voltage Switching (ZVS) Operation

The resonant switch for the ZVS operation is provided by the connection of a resonant capacitor ( $C_R$ ) across the switch, as shown in Figure 4.b. This resonant capacitor may be the internal parasitic capacitance of the semiconductor switch or an externally added capacitor if required. The turn-off of the switch is completed with low switching power loss due to  $C_R$ , which slows down the rise of  $V_S$ , hence the switch is completely turned-off ( $I_S$  is reduced to zero) before  $V_S$  reaches a significant value. The turn-on of the switch for ZVS operation is carried out by the resonance of capacitor  $C_R$  with an external inductor, which is connected to the resonant switch either in series or parallel. Due to resonance,  $I_S$  starts to increase after  $V_S$  is reduced to zero, resulting in a ZVS operation during turn-on switching interval. The semiconductor switching device parasitic output capacitance can be utilized for ZVS operation. Thus, except for specific operating conditions (such as cases where switch dead-times become a limiting factor), there is no need for external circuit components. Otherwise, additional capacitors are connected in parallel to the switches to complete the circuit for ZVS operation.

#### ZVS Benefits

- Zero power “Lossless” switching transitions
- Reduced EMI / RFI at transitions
- No power loss
- No higher peak currents
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and component L & C
- Reduced gate drive requirements (no “Miller” effects)
- Short circuit tolerant

## V. INTERLEAVED BOOST CONVERTER

The conventional boost topology is the most popular topology for PFC applications. It uses a dedicated diode bridge to rectify the AC input voltage to DC, which is then followed by the boost section. In practical applications as the power level increases, the diode bridge losses become significant, so dealing with heat dissipation in a limited surface area is important, particularly from an efficiency point of view. Therefore, the conventional PFC boost is limited to low to medium power range.

### INTERLEAVED BOOST CONVERTER

A two-phase interleaved boost converter is usually employed for high power applications with high conversion gain. Interleaving brings additional benefits such as reducing ripple currents in both the input and output circuits. Higher efficiency is realized by splitting the output current into ‘n’ paths, substantially reducing power losses and inductor losses. The advantages of interleaved boost converter are minimizing current ripple, increasing efficiency, making faster transient response, reducing electromagnetic emission and improving reliability. The gating pulses of the two phases are shifted by  $360/n$ , i.e.,  $360/2$  for  $n = 2$ , which is 180. Figure-5 shows a two-phase interleaved boost converter.

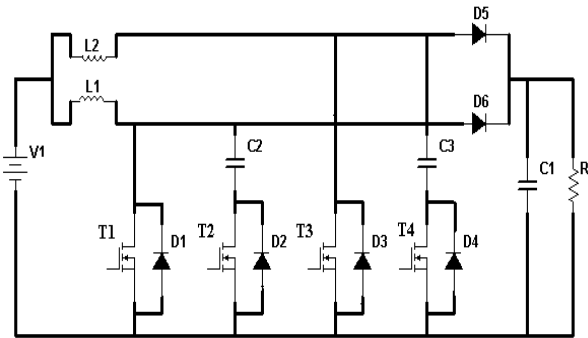


Fig. 5. Interleaved Soft Switched Boost Converter.

### Selection of Boost Power Stage Components

The interleaved boost converter design involves the selection of the inductors, the input and output capacitors, the power switches and the output diodes. Both the inductors and diodes should be identical in both channels of an interleaved design. In order to select these components, it is necessary to know the duty cycle range and peak currents. Since the output power is channeled through two power paths, a good starting point is to design the power path components using half the output power. The following four parameters are required to calculate the power stage components.

1. Input Voltage Ranges of  $V_{in(min)}$  and  $V_{in(max)}$
2. Nominal Output Voltage of  $V_{out}$
3. Maximum Output Current of  $I_{o(max)}$
4. Integrated Circuit used to build the interleaved boost converter.

### 2. Determine the Maximum MOSFET Switch Current

The first step to calculate the MOSFET switch current is to determine the duty cycle,  $D$ , for the minimum input voltage. The minimum input voltage is used because this leads to the maximum switch current.

Calculation of Duty Cycle:

$$\text{Duty Cycle } D = \frac{1}{2} \left( 1 - \frac{V_{in(min)} \times \eta}{V_{out}} \right) \quad (1)$$

$V_{in(min)}$  = Minimum input voltage

$V_{out}$  = Desired output voltage

$\eta$  = Efficiency of the converter, e.g. estimated 99%

The next step to calculate the maximum switch current is to determine the inductor ripple current.

Calculation of inductor ripples current:

$$\text{Inductor Ripple Current } \Delta I_L = \frac{V_{in(min)} \times D}{f_s \times L} \quad (2)$$

$V_{in(min)}$  Minimum input voltage

$D$  Duty Cycle derived in Equation (1)

$f_s$  = Minimum switching frequency of the converter

$L$  = Approximate inductor value for calculation

The next step is to calculate the maximum output current of the converter.

Maximum Output Current is

$$I_{o(max)} = \left[ I_{Smin} - \frac{\Delta I_L}{2} \right] \times [1 - D] \quad (3)$$

$I_{Smin}$  = minimum value of the current limit of the MOSFET switch.

$\Delta I_L$  = inductor ripple current calculated in Equation 2.

$D$  = duty cycle calculated in Equation 1.

A higher inductance leads to reduce the ripple current and therefore increases the maximum output current.

The maximum MOSFET switch current is

$$I_{Smax} = \frac{\Delta I_L}{2} + \frac{I_{o(max)}}{1 - D} \quad (4)$$

$\Delta I_L$  = Inductor ripple current calculated in Equation 2

$I_{o(max)}$  = maximum output current calculated in Equation 3.

$D$  = duty cycle calculated in Equation 1

This is the peak current in which the inductor, the switches and the external diodes has to withstand.

### 3. Selection of Power Inductor for DC - DC Converter Switching frequency

Suitable core materials of power inductor are iron powder, ferrite and super flux for the converters operating in the range of 30 KHz to 100 KHz switching frequency.

Inductance value

The inductance value can be calculated as

$$\text{Inductance } L = \frac{V_{in} \times (V_{out} - V_{in})}{\Delta I_L \times f_s \times V_{out}} \quad (5)$$

Where,  $V_{in}$  = Input voltage,  $V_{out}$  = Expected output voltage.

$\Delta I_L$  = Estimated inductor ripple current,

$f_s$  = Switching frequency of the converter

It is noticed that selection of higher inductance value leads to smaller ripple currents and selection of lower inductance value leads to higher ripple currents. Besides the switching frequency, the ripple current is equally important when minimizing the power loss of the inductor. Also, consider a good estimation for the inductor ripple current is 20% to 40% of the output current.

Inductor ripple current

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{0\max} \times \frac{V_{out}}{V_{in}} \quad (6)$$

Inductor current ratings

The current ratings for power inductor can be calculated in terms of DC load current and input ripple current.

Nominal current of the inductor

$$I_N = \left( \frac{V_{out}}{V_{in}} \right) \times I_{out} \quad (7)$$

$$\text{Maximum coil current } I_{\max} = 2 \times I_{in} \quad (8)$$

The nominal current for power inductor is referred commonly to self heating with DC current at the temperature of +40°C.

DC Resistance

Selection of power inductor with the minimum possible DC resistance is important after the calculated values for inductance L and inductor currents. The DC resistance value is useful in finding wire heating losses for minimizing the power loss of the inductor. Choosing higher inductance value leads to increase the value of DC resistance and lower inductance value leads to decrease the value of DC resistance. Preferably, use of shielded inductor with same inductance value leads to decrease the value of DC resistance.

It is advisable to keep Electro Magnetic Compatibility (EMC) for critical applications, the shielding of power inductor avoids uncontrolled magnetic coupling due to air gap exists in the windings with adjacent conductor tracks or components. It is highly preferable for selecting power inductor of small size, high energy storage density and low DC resistance.

### 4. Output Capacitor Selection

Best practice is to use low Equivalent Series Resistance (ESR) capacitors to minimize the ripple on the output voltage.

Ceramic capacitors are a good option if the dielectric material is X5R or better.

The following equations can be used to regulate the output capacitor values for a desired output voltage ripple.

$$\text{Output Capacitance is } C_0 = \frac{I_0 \times D}{f_s \times \Delta V_{out}} \quad (9)$$

$I_0$  = Necessary output current,  $D$  = Duty cycle

$f_s$  = Switching frequency of the converter,

$\Delta V_{out}$  = Recommended output voltage ripple.

The ESR of the output capacitor adds some more ripple, given with the equation:

$$\Delta V_{out(ESR)} = \text{ESR} \times \left[ \frac{I_{0(\max)}}{1-D} + \frac{\Delta I_L}{2} \right] \quad (10)$$

$\Delta V_{out(ESR)}$  = Additional output voltage ripple due to capacitors ESR.

ESR = Equivalent series resistance of the used output capacitor.

$I_{0(\max)}$  Maximum output current of the converter

$D$  = duty cycle calculated with Equation 1

$\Delta I_L$  Inductor ripple current from Equation 2 or Equation 6.



## 5. Rectifier Diode Selection

The forward current rating should be equal to the maximum output current to reduce losses.

$$I_f = I_{o(max)} \quad (11)$$

$I_f$  = Average forward current of the rectifier diode

$I_{o(max)}$  = maximum output current

The power dissipation of the diode

$$P_D = V_f \times I_f \quad (12)$$

$I_f$  = average forward current of the rectifier diode

$V_f$  = forward voltage of the rectifier diode

## 6. Calculation of Coupling Coefficient K:

The conduction losses of the main switches and reverse recovery losses of the diodes are greatly reduced by choosing the value of  $K = 0.98$ .

## VII. CONCLUSION

This paper has investigated the basic design aspects of interleaved boost. The proposed topology has the advantages of ZVS during the turn on transition and ZCS during the turn off transition. By means of interleaving technique, with the addition of two auxiliary cells, the performance of the converter can be enhanced. The soft switching approach helps to reduce the switching loss and improves the efficiency. Furthermore, the reverse-recovery current of the diode are greatly reduced compared to hard switching converters. The design equations for IBC have been presented in detail. The choice of number of phases and the relation with the input current and output voltage ripple is also discussed. This design will be helpful for the telecom engineers to design the power supply component. The proposed IBC seems to be a suitable topology for telecommunication systems.

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