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# High Speed Fault Tolerant Reversible Vedic Multiplier

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*Abstract*— ***Multiplier is the most widely used arithmetic unit, having great importance in the digital world. For example- Digital Signal Processing, Processor and Quantum Computing etc. The Multiplier is the slowest and having a complex structure. In this paper a 4x4 bit high speed and fault tolerant multiplier architecture is proposed .The speed of the multiplier is enhanced with the help "Urdhva Tiyagbhayam" aphorisms from the ancient Vedic Mathematics. Further the architecture of the multiplier is implemented using the Fault Tolerant Reversible Gates which exhibits a fault tolerant property by preserving the parity. Hence the parity checking method is used to find out the error and correction. Finally the Partial Product of the multiplier is added with the help of fault tolerant Carry look ahead adder. The coding is written in Verilog .While synthesis and simulation is performed using Xilinx 14.7i.***

***Keywords— Fault Tolerant Reversible logic gates, Carry look ahead adder ,Vedic method***

## I. INTRODUCTION

As the technology is scaling down from micro scale to nano scale. At such scale a new field is evolved is called quantum computing. Quantum computations perform reversible operation, mean the information is conversed and performs certain task in nanosecond. [1]These are the main motivation to develop a high speed multiplier using reversible logic gates. In order to implement a high speed multiplier and Vedic algorithm is applied .Because it perform simple operation and yield result quickly. The multiplication process involves two step generation of partial product and addition of partial product, these two steps are concurrently perform by the Urdhva Triyagbhyam algorithm of Vedic Mathematics [5]

This paper proposes the implementation of fault tolerant reversible Vedic multiplier, with the aim to develop a high speed multiplier with Vedic method and the architecture of multiplier is implemented with fault tolerant reversible gate in order to improves the reliability, reduces area. The paper is organized as follows: Section 2 describes Reversible logic, Section 3 Urdhav Tiryakbhayam aphorism, Section 4 Fault Tolerant Carry Look Ahead Adder Section 5 Proposed 4x4 bit Fault Tolerant Reversible Vedic Multiplier Architecture Section 6 shows the Result and Comparison and Section 7shows the Conclusion.

## II. REVERSIBLE LOGIC

### A. *Importance of Reversible Logic*

Reversible logic perform reversible computation means that the input can be recovered back from the output and the output can also be obtained from the input . Hence the reversible logic circuit are also called as the Information loss-less logic. Reversible logic can be of two types they are Basic Reversible gate and Fault Tolerant Reversible Gates. Reversible gate are those gates having the same number of the input lines and the output line. While Fault tolerant Reversible gate are also known as the parity preserving reversible gate which performs reversible computation as well as the preserve the parity at the input side as well as at the output side.[12] Some of the Fault Tolerant Reversible Gate are shown in the below:

#### 1. *Double Feynman Gate*

The double Feynman gate is a 3*3 gate are shown in the figure1. The input vector is I(A,B,C) and output vector is O( P,Q,R). The input parity is same as the output parity .Quantum Cost of F2G is equal to 2.

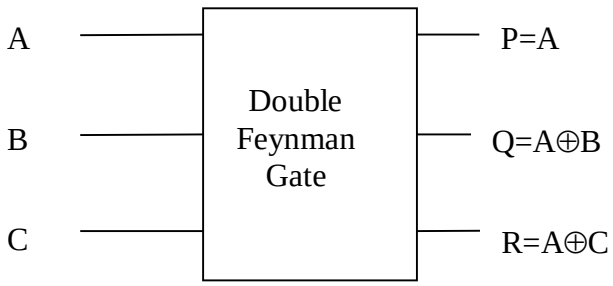


Figure 1- Feynman Gate

 

### 2. *Islam Gate(IG)*

The Islam gate is a 4*4 gate are shown in the figure 2. The input vector is I(A,B,C,D) and output vector is O( P,Q,R,S). The input parity is same as the output parity and Quantum Cost of F2G is equal to 7. It can perform AND,EX-OR function.

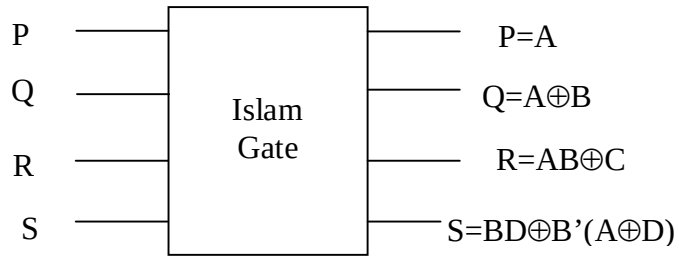


Figure 2- Islam Gate

### 3. *NFT Gate*

The NFT gate is a 3*3 gate are shown in the figure 3. The input vector is I(A,B,C,D) and output vector is O( P,Q,R,S). The input parity is same as the output parity. Quantum Cost of NFT is equal to 5. It can perform NOT, OR , XOR,NAND,AND,EX-OR function.

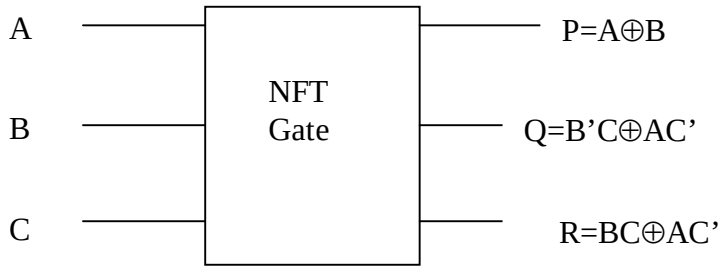


Figure 3- NFT Gate

## III. **URDHVA TRIYAGBHAYAM APHORISMS**

Urdhva Tiryakbhayam(UT) sutra is the multiplication formula from the ancient Vedic mathematic which suits for the multiplication of decimal number, hex as well as for the binary number. The multiplication of two decimal number is shown in the figure 4. This features of UT algorithm compatible with the digital systems. The UT provides the fast computation because the partial product and their sums are calculated parallel. The Sanskrit words Urdhav means vertical and Tiryagbhyam" means "crosswise" in English..These algorithm performs crosswise and vertical operations between the two numbers. The procedure is adapted for the multiplication is based on the concept in which generation of the partial products and additions are done concurrently which increases the speed of multiplication operation.[7]

 

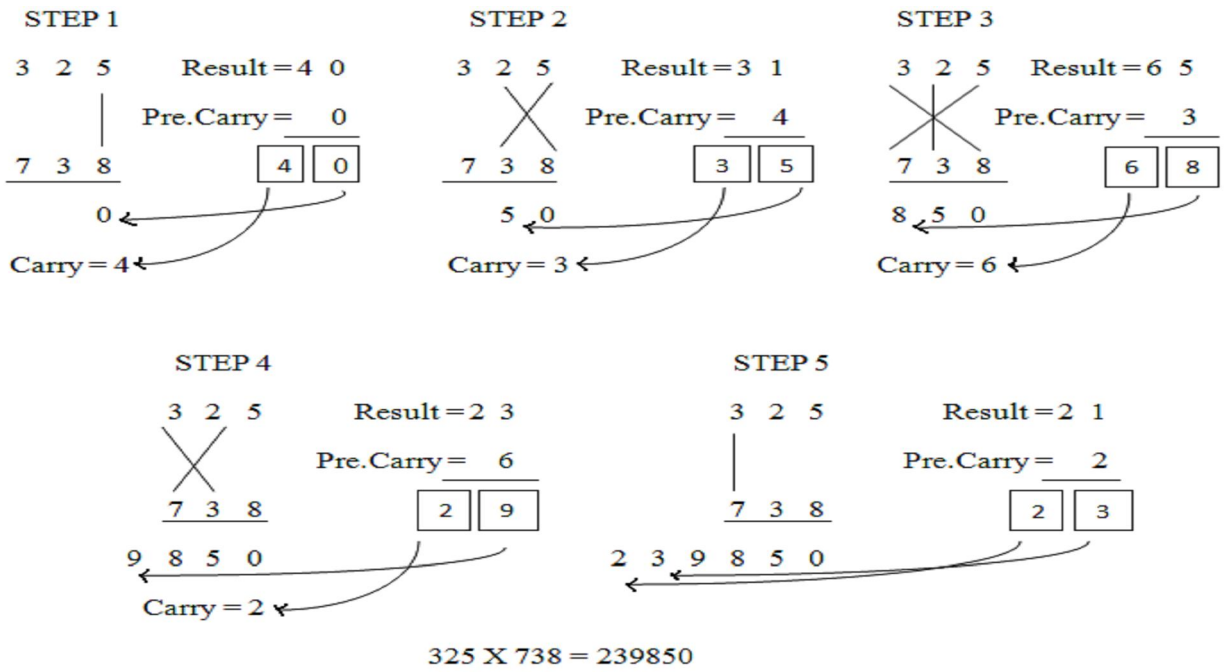


Figure 4- Urdhva Tiryakbhyam multiplication of the two decimal number

## IV. FAULT TOLERANT CARRY LOOK AHEAD ADDER

Carry-look ahead adder is the fastest adder among the all adders. It generates carry bit in advance before it generates the sum, which reduce computation time to obtain final results.[10] Here the Carry look ahead adder is implemented using the New Fault Tolerant gate (NFT ) gate and Double Feynman gate. Fault tolerant carry look ahead adder is used to add the partial product of the Vedic multiplier blocks .The 2-bit fault tolerant carry look ahead adder is shown in the figure 5.

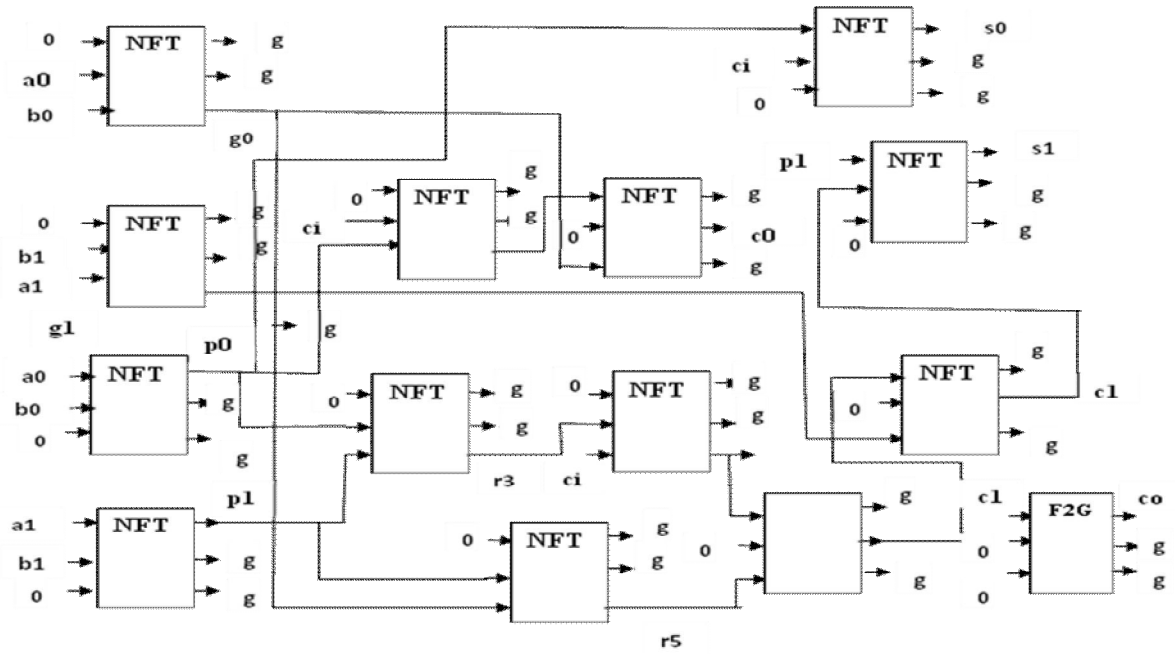


Figure 5- 2-Bit Fault Tolerant Carry Look Ahead Adder.

## V. IMPLEMENTATION OF PROPOSED MULTIPLIER ARCHITECTURE

*A . 2x2 Fault tolerant Reversible Vedic Multiplier*

To implement 2x2 –bit Fault Tolerant Reversible Vedic Multiplier. For multiplication algorithm Urdhva tiryakbhyam is applied between the multiplier and multiplicand of 2-bit A0A1 and B0B1. The result obtained in 4-bit say P0,P1,P2 and P3. The logical expression are below:

 

P0=A0.B0
P1=A1.B0 xor A0B1
P2=A0.A1.B0.B1 xor A1B1
P3=A0.A1.B0.B1(carry generated from P2)

The computational steps performed by the Urdhva Tiryakbhyam for the 2 bits are as follows In first step P0 is obtained by vertical multiplication of A0 and B0. In second step P1 is obtained by the crosswise multiplication and addition of the partial products they are A1B0 and A0B1.In the third step P2 is obtained by the multiplication of A1 and B1. Finally P3 is obtained is nothing but the carry generated from the calculation of P2. P3 represent the final result term.
These logical expression is implemented using fault tolerant reversible gates (also known as parity preserving gates). Fault tolerant reversible gate exhibits a fault tolerant property. If the system itself composed of fault tolerant gate then it exhibits a fault tolerant property because it preserves a parity and provides a fault detection at the primary output and no intermediates checking is required . The fault tolerant reversible implementation of above logical expression uses fault tolerant gates or parity preserving gates they are four double Feynman gate, four New fault Tolerant Gate (NFT) and Two Islam Gate(IG) to implement 2x2 bit Vedic multiplier is known as 2x2 bit Fault tolerant Reversible Vedic Multiplier which is shown in the figure 6.

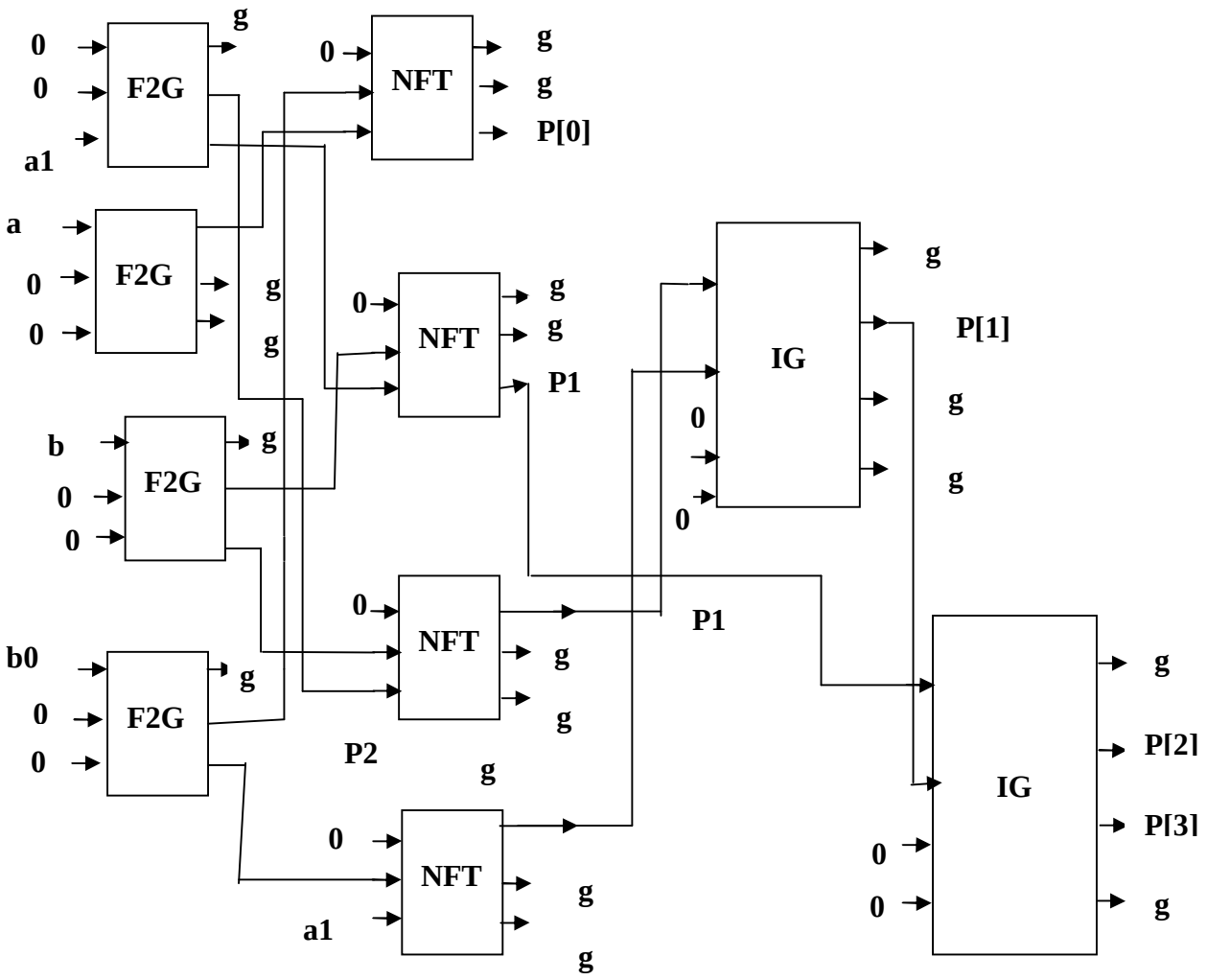


Figure 6-2x2 bit Fault Tolerant Reversible Vedic Multiplier

 

*B. 4x4 Fault Tolerant Reversible Vedic Multiplier*

To design and implement 4x4 bit multiplier, An Vedic Algorithm is applied between the four bit of multiplier and multiplicand say A[3:0],B[3:0] and produce the multiplication result in P[7:0] bit. The four 2-bit fault tolerant reversible vedic multiplier is required to implement an 4-bit multiplier. According to the Urdhva Tiryakbhyam the multiplier and multiplicand is split into four module of each 2-bits. The output of the first and second 2x2 bit multiplier module are concatenated with the 2-bit and introduce it as an input to the 6-bit fault tolerant carry look ahead adder. Similarly the output of the third and fourth 2x2 bit multiplier module is concatenated with 2-bit and introduce as an input to an another 6-bit fault tolerant carry look adder. Finally the output from these two fault tolerant carry look ahead adder is again concatenated with 2-bit, and introduce as the input to the 8-bit carry look ahead adder to produce an 8-bit multiplication output P[7:0]. The block diagram of the 4x4 Bit Fault tolerant Reversible Vedic multiplier is shown in the figure 7.

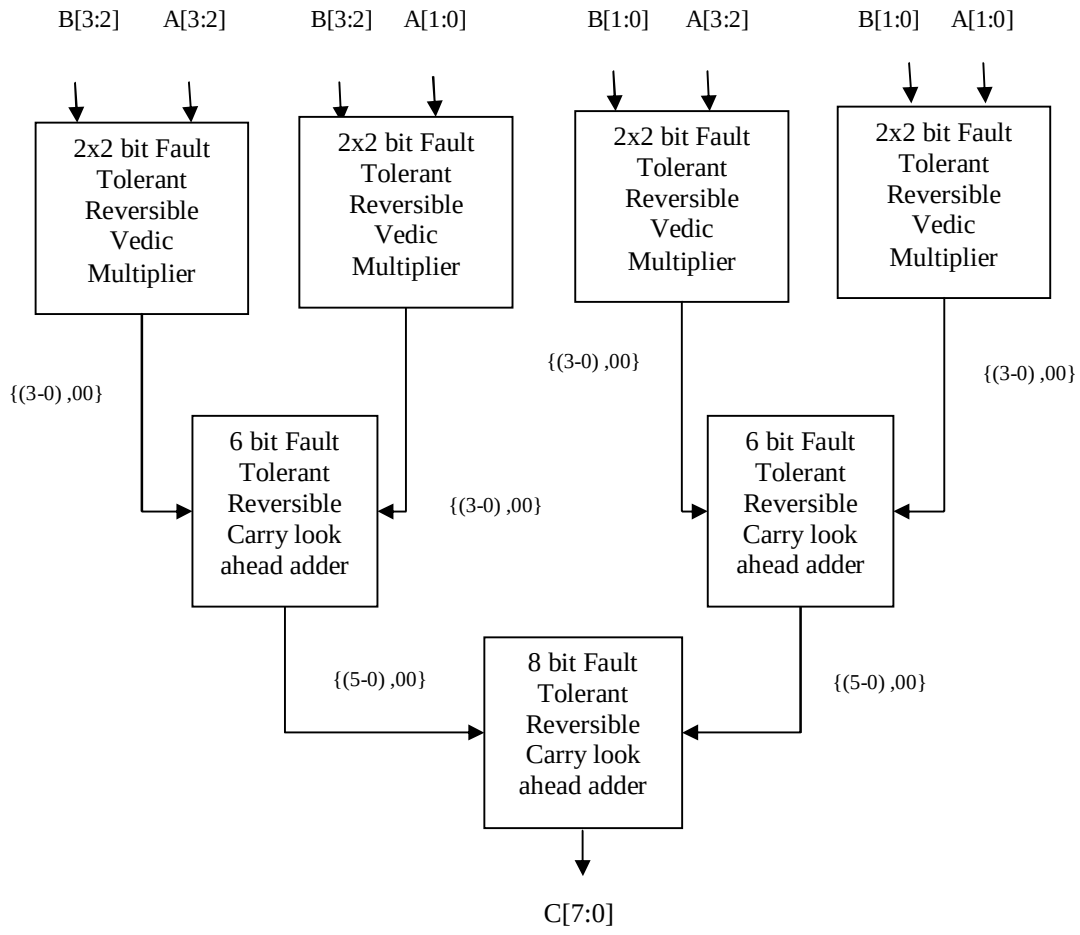


Figure 7- Block diagram of the 4x4 Bit Fault Tolerant Reversible Vedic multiplier

## VI . RESULT AND COMPARISON

In this paper 4x4 bit Urdhav Tiryakbhyam multiplier using fault tolerant reversible gates are designed in Verilog and the synthesis and simulation was done using Xilinx14.7i. The synthesis result obtained for the Proposed Fault tolerant Reversible Vedic multiplier and simulation results and RTL synthesis are shown in Figures 8 and 9 respectively. The device utilization summary of 4x4 bit fault tolerant reversible Vedic multiplier for Xilinx, Virtex 6-family is shown below:

Device Utilization Summary**:** Selected Device : 3s500efg320-5.
Number of LUT Flip Flop pairs used: 28
Number with an unused Flip Flop: 28 out of 28 100%
Number with an unused LUT: 0 out of 28 0%
Number of fully used LUT-FF pairs: 0 out of 28 0%

 

The simulation result is obtained for the Proposed Fault Tolerant Reversible Vedic multiplier for verification is shown in figure 12 .In behavioral simulation test is performed for the given input bits-

a) For 4x4 bit parity preserving reversible Vedic multiplier input ,multiplier a="12 and multiplicand b= "12" and we get 128-bit output c= "144" . Similarly another input is applied where multiplier a= "18" and multiplicand b= "18" also we get the output in 128 bit , c= 324.

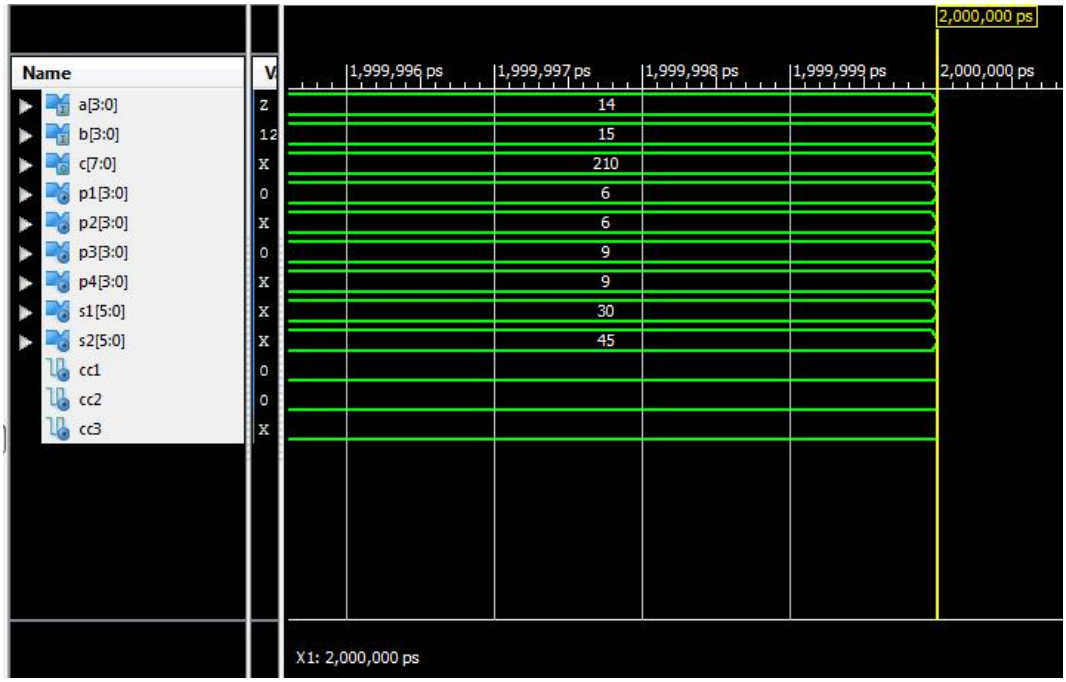


Figure 8:Simulation Result of 4x4 Bit Fault Tolerant Reversible Vedic Multiplier with carry look ahead adder

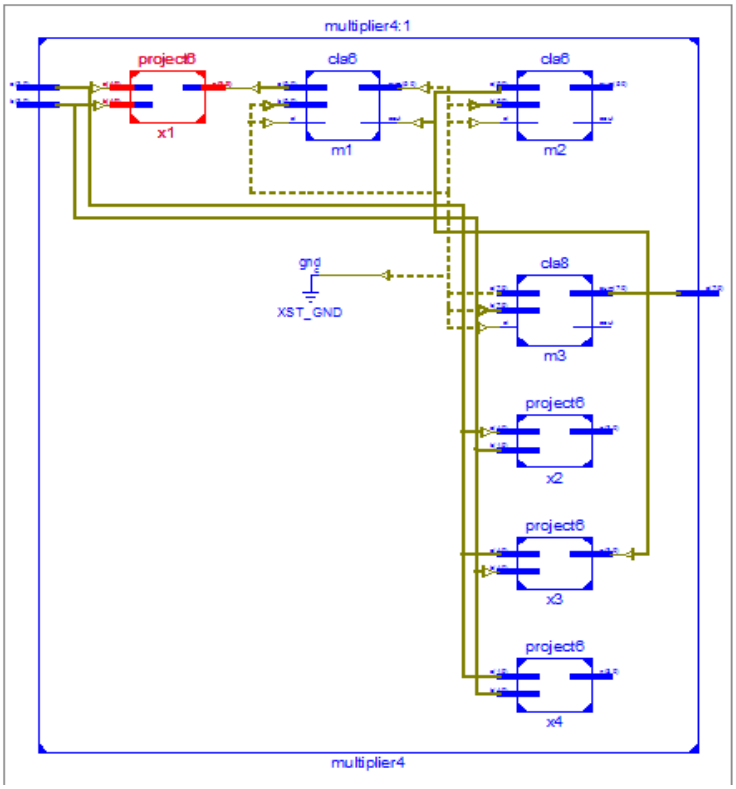


Figure 9 - RTL Schematic of Proposed 64x64 Fault Tolerant Reversible Vedic multiplier

 

Table I shows the comparisons of Proposed 4x4 bit Fault tolerant Reversible Vedic Multiplier using carry look ahead adder in terms of computational path delays (ns) and fault tolerant property.

Table -I

| For 4x4 –bit Multiplier | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **S.No** | **Parameter** | **Reversible Vedic multiplier With Proposed Design I [19]** | **Reversible Vedic multiplier With Proposed Design II [19]** | **Reversible Vedic Multiplier With ripple carry adder [14]** | **Vedic Multiplier with carry save adder** | **Vedic Multiplier with ripple carry adder [15]** | **Vedic Multiplier with carry look ahead adder [15]** | **Proposed Fault Tolerant Vedic reversible using carry look ahead adder** |
| **1.** | **Delay (ns)** | **19.109ns** | **17.192ns** | **16.910ns** | **13.102ns** | **15.995ns** | **13.786ns** | **3.614ns** |
| **2.** | **Fault Tolerant Property** | **No** | **No** | **No** | **No** | **No** | **No** | **Yes** |

Table I-Comparisons of Proposed 4x4 bit Fault Tolerant Reversible Vedic Multiplier using carry look ahead adder with other multipliers

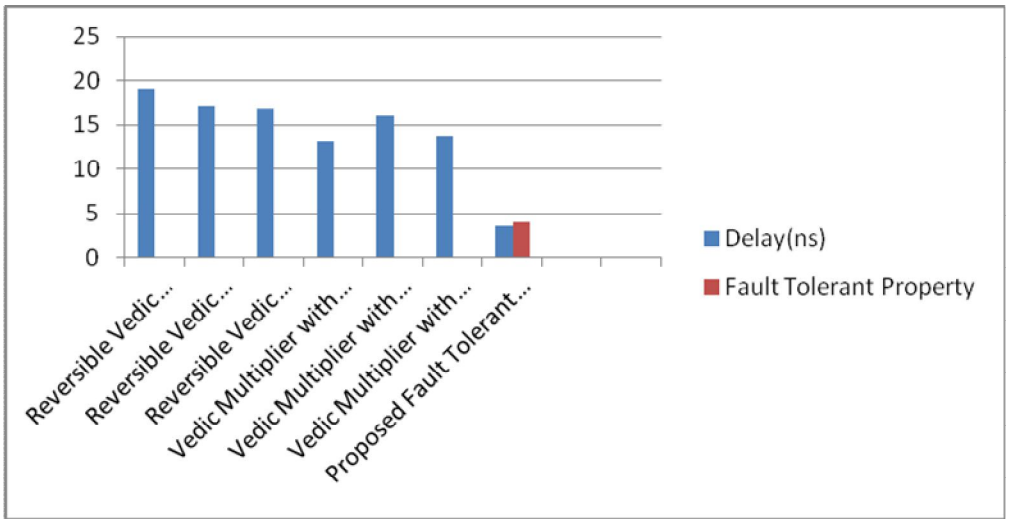


Chart-I Comparison Between the fault tolerant Reversible Vedic Multiplier and other existing multiplier

## VI. CONCLUSIONS

This paper presented a high speed multiplier using Urdhva tiryakbhayam algorithm for multiplication based on Vedic mathematics and the partial product addition is done by the fault tolerant carry look ahead adder which offered fast computational speed. While architecture of multiplier is implemented using fault tolerant reversible gate . The Proposed 4x4 Fault tolerant Reversible Vedic Multiplier have minimum path delay and fault tolerant capability when compared to other multipliers.

In future, adaptive LMS filter can be designed using fault tolerant reversible Vedic multiplier which provide faster computational speed, These multiplier used in quantum computer ,as quantum computing perform computation in reversible manner.

 

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