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Design and Simulation of 2–Bit Comparator Using SET Based Logic Circuits

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Abstract— Single electron devices have ultra-low power consumption and high integration density which makes them promising candidates as basic circuit elements for the next generation ultra-dense VLSI and ULSI circuits. In this paper, design, simulation and analysis of 2-bit comparator using single-electron tunnelling technology based logic circuit is presented. The logic operation of the circuit was simulated and stability analysis was carried out for various temperatures using SIMON software.

Keywords— Comparator, SET, tunnel junction, CMOS, SIMON, stability

I. INTRODUCTION

During the last decade the feature size of MOS based circuits has dramatically decreased and the number of transistors has increased. With the dominance of CMOS technology over decades under the rules of Moore's law, researchers estimate that its further limitation of size will reach a lower limit within the next 10 to 15 years. However, the power consumption of the chip monotonically increases as the number of transistors increases. This will limit the integration scale because the power consumption will exceed the cooling limit. The Single Electron Transistor (SET) is expected to be a key device for future extremely large-scale integrated circuits because of its ultralow power consumption and small size. The SET has a great potential for low-power yet high-performance signal processing and hence for furthering the multimedia society. SET is a key element of current research area of nanotechnology which can offer low power consumption and high operating speed.

II. 2-BIT COMPARATOR

In digital system, comparison of two numbers is an arithmetic operation that determines if one number is greater than, equal to, or less than the other number. So comparator is used for this purpose[5]. Magnitude comparator is a combinational logic circuit that compares two numbers, A and B, and determines their relative magnitudes as shown in Figure.1. The outcome of comparison is specified by three binary variables that indicate whether **A>B, A=B, or A<B.**

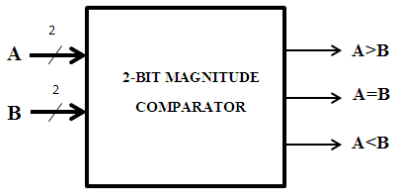


Figure 1: Block Diagram of 2-Bit Comparator

The truth table of a 2 bit comparator is given in TABLE 1 and the Boolean logic based implementation is shown in Figure 2.

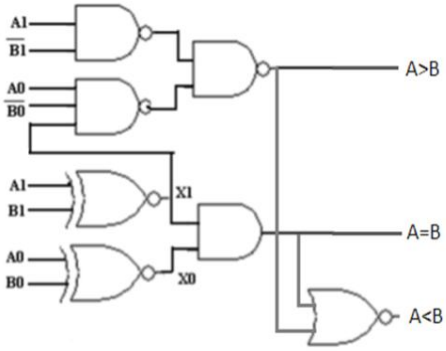


Figure 2: Logic Diagram of 2-bit Comparator

TABLE 1
2-BIT COMPARATOR TRUTH TABLE

INPUT				OUTPUT		
A1	A0	B1	B0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

III. BASIC ELEMENTS OF 2-BIT COMPARATOR

The basic elements used in 2-bit comparator are AND gate, OR gate, XOR gate and NOT gate which are designed using SET technology.

A. NOT Gate

The inverter is a fundamental building block of SET technology, which bears considerable resemblance to standard CMOS logic. The single electron inverter is shown in Figure 3. The circuit consists of five islands bounded by four tunnel junctions.

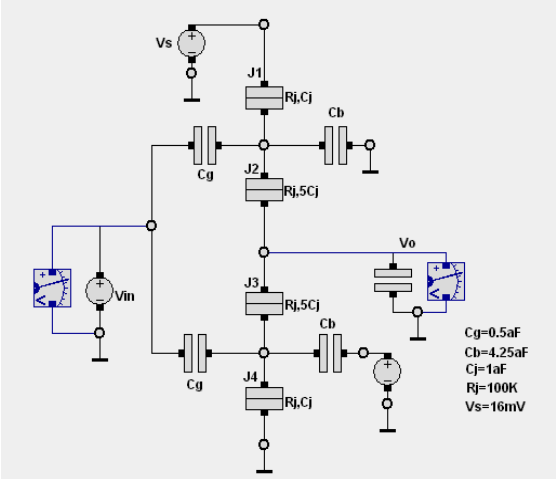


Figure 3: SET based Inverter

B. AND Gate

AND gate gives high output only when both the inputs are high. The Single electron AND gate is shown in Figure 4. The circuit consists of eight islands bounded by five tunnel junctions.

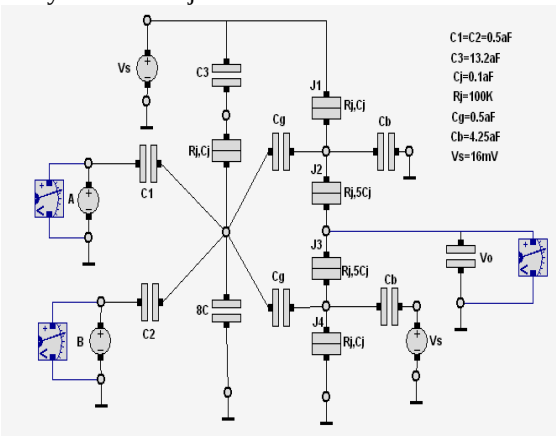


Figure 4: SET based 2-input AND gate

C. OR Gate

OR gate gives high output when any of the input is high or both the inputs are high. The Single electron OR gate is shown in Figure 5. The circuit consists of eight islands bounded by five tunnel junctions.

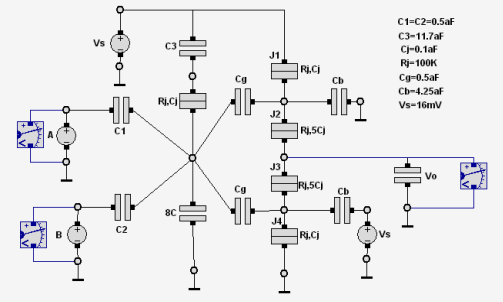


Figure 5: SET based 2-input OR gate

D. XOR Gate

The XOR gate is a digital logic gate that implements an exclusive OR i.e., a high output results if one, and only one, of the inputs to the gate is true. If both inputs are low, or both are high, a low output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. The Single electron XOR gate is shown in Figure 6. The circuit comprises eleven islands bounded by six tunnel junctions.

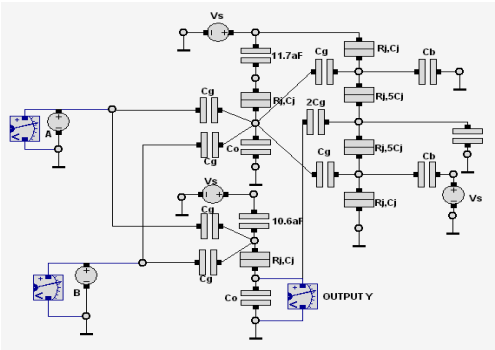


Figure 6: SET based 2-input XOR gate

E. Single Electron Two Bit Comparator

The single electron 2 bit comparator is designed and simulated as shown in Figure 7. The circuit comprises of 165 islands N1, N2, N3….N165 bounded by 69 tunnel junctions. The capacitance of J junctions is 0.1×10^{-18}F and their resistances are 1×10^{5} Ohm. The voltage V_{dd} is constant and its value 16 mV.

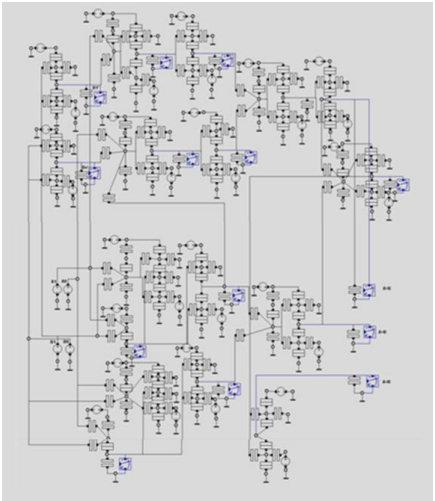


Figure 7: SET based 2-bit comparator

IV. SIMULATION RESULTS AND ANALYSIS

The logic operations of basic logic gates are first examined independently by simulation using Monte Carlo simulation software SIMON. The input-output waveforms of inverter are shown in Figure 8. The input output waveform of AND gate, OR gate and XOR gate are shown in Figure 9, Figure 10 and Figure 11 respectively. Figure 12 shows the simulation result of 2-bit comparator [2, 3]. The results obtained from the simulation are found to be the desired output as per the truth table shown in TABLE 1.

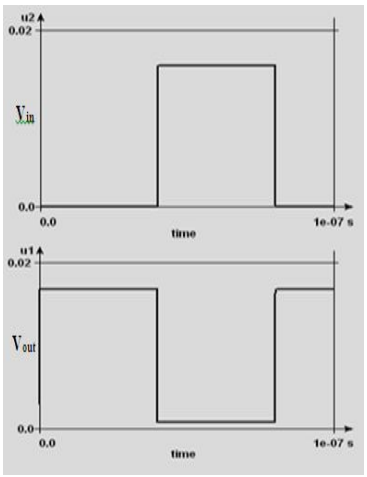


Figure 8: Simulation result of Inverter

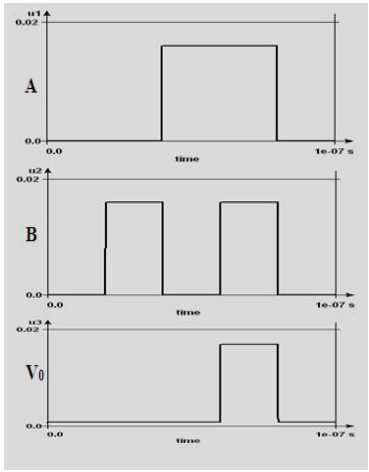


Figure 9: Simulation result of AND gate

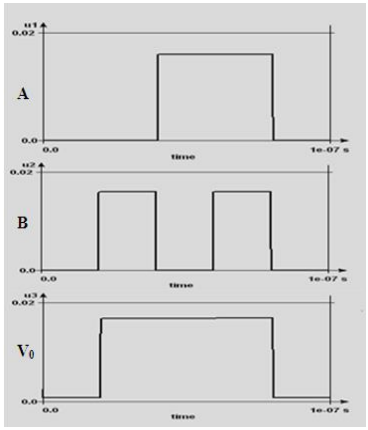


Figure 10: Simulation result of OR gate

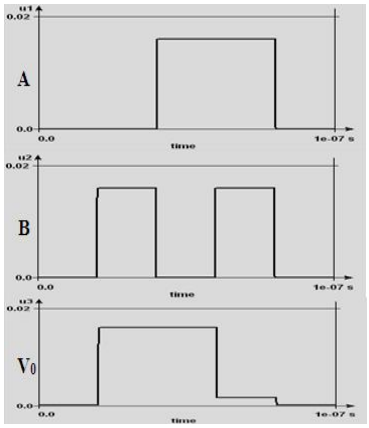


Figure 11: Simulation result of XOR gate

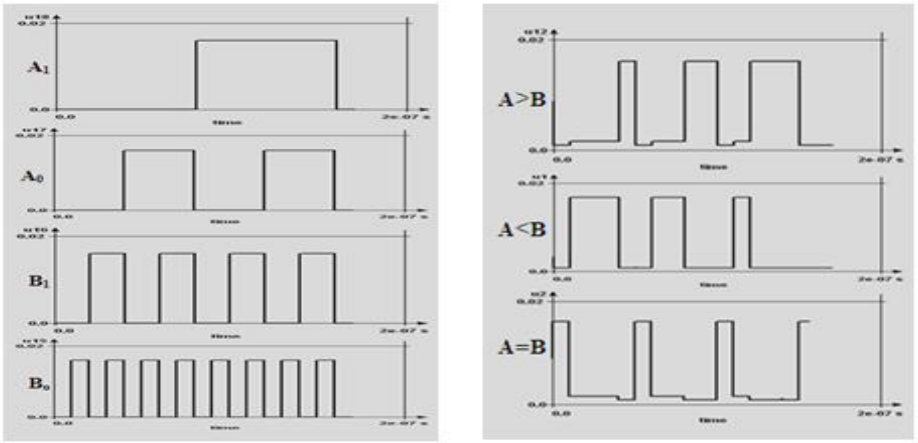
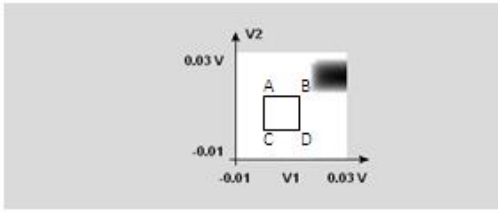


Figure 12: Simulation Result of 2-Bit Comparator

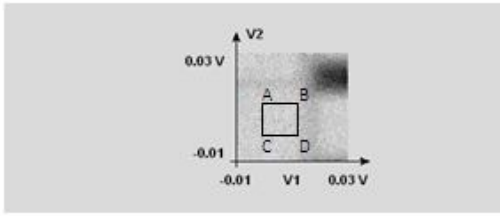
Stability Analysis

The stability of 2 bit comparator has been tested using SIMON software. The stability plot of 2 bit comparators at 0 K, 10 K and 20 K is shown in Figure 13. The local minima of the circuit's free energy correspond to a stable condition and these points are coloured white. The local maxima of the circuit's free energy correspond to unstable points and they are coloured black. The points which are coloured grey correspond to small currents that run through the junction. The points A, B, C and D correspond to the input control signal vectors [1,0], [1,1], [0,0] and [0,1] respectively. All the points corresponding to the control input vectors are found to be located in the stable white and grey portions of the stability plot[8].

(a)



(b)



(c)

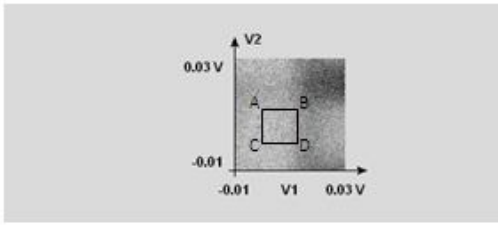


Figure 13: Stability plot of 2-bit comparator with A [1, 0], B [1, 1], C [0,0] and D[0,1] points for (a) 0K (b) 10K (c) 20K

V. CONCLUSION

The design, simulation and analysis of 2-bit comparator using SET based logic gate is presented. The circuit compares a pair of 2 bit inputs and produces outputs A>B , A=B and A<B. The performance of the proposed circuit is verified by simulation using SIMON2. The stability of the circuits is tested at different temperatures. All the points that correspond to the input vectors are found to be located in the stable white portion of the stability plot. The influence of thermal fluctuation with the increase in temperature is observed. With the increase in temperature the grey and black points increases.

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