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SIMULATION OF A BUCK CONVERTER CONTROLLER BASED ON A HARDWARE AND SOFTWARE PSM MODE CONTROL

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Abstract— A DC-DC converter is often controlled by a circuit based on analog electronic components and logic gates. In this study we will compare the control of the converter provided by an electrical circuit based on conventional electronic components and a control provided by a programmable circuit. The control mode chosen is the pulse skipping modulation mode (PSM). It is a relatively simple and easily programmable mode. The controlled DC-DC converter is a Buck converter. The control program, implanted on a microcontroller dsPIC is translated directly from a diagram realized under SIMULINK using the tool MPLAB SIMULINK BLOCKSET for MATLAB. The use of the ISIS/Proteus simulator allowed us to compare the simulation results obtained from the hardware control and those obtained from the software control.

Keywords — Buck Converter, dsPIC , ISIS/PROTEUS, MPLAB SIMULINK Blockset, PSM mode control.

I. INTRODUCTION

DC Static converters are designed mostly based on power electronics components used as switches. They are equipped with a control circuit which must act on the opening or closing of the switch according to a well-defined protocol and frequency. These control devices are implemented in the form of analogue or digital circuits. Recently, we are moving towards a programmed control managed by a programmable logic circuit. The advantage of this method is its simplicity and flexibility compared to a conventional control. The work presented aims to make a comparison between the programmed control and the control based on conventional electronic components. The selected control mode is PSM (Pulse Skipping Modulation). It is a relatively simple mode to carry out electrically and easily programmable on a microcontroller. The controlled converter is a Buck converter operating in continuous conduction mode (CCM). The control will be carried out initially in the form of a logic circuit clocked by an external clock. This circuit will then be replaced by a microcontroller of type dsPIC on which we will implement the control program using a tool provided by the manufacturer of the microcontroller and integrated with MATLAB. The practical circuit representing the converter and the dsPIC containing the control program will be simulated under ISIS/Proteus and the results of this simulation will be compared with those obtained from control system based on conventional electronic components under the same conditions.

II. BUCK CONVERTER AND PSM CONTROL

A. Buck Converter

The converter consists of a switch (MOSFET), a diode, an inductance coil L and a capacitor C with a resistive load as shown in figure-1.

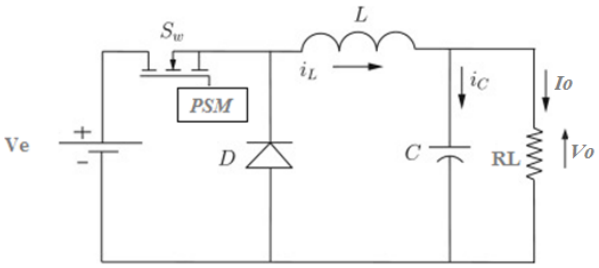


Figure-1. Buck Converter

The buck converter is controlled by a PSM type impulse control device [1],[2].

The adopted mode of operation is the continuous conduction mode (CCM) [3]-[6].

The PSM regulator which will supply the pulses to the switch will act on the converter according to the result of comparison of the reference voltage (V_{ref}) and the output voltage (Vo) taken at the load R_L. It is introduced in the form of a MATLAB function which will apply to the switch (MOSFET) a clock signal H [7]. The clock frequency f_h and the duty cycle α remain fixed. When the load R_L voltage Vo is lower than the reference voltage Vref, the pulse train is sent to the switch, which will result in an increase in voltage and current across the load, that is the charging period of the capacitor. When Vo exceeds Vref the pulses are blocked and the opening of the switch causes discharge of the capacitor and consequently the decrease of the voltage across the load. When the voltage Vo becomes lower than the reference voltage (Vref), the pulse train is applied again to the switch and the voltage Vo increases. Thus, when the steady state is established, the voltage Vo will oscillate periodically around the reference voltage (Vref) with a ripple whose amplitude will be greater or less according to the value of the load resistor R_L.

B. Modeling the PSM Function

When the steady state is established after a transient phase, the clock signal with period T_h (frequency f_h)and duty cycle α will be applied to the MOSFET when Vo < Vref (charge period of the capacitor) and blocked in the opposite case (period of discharge). During the charging period, the MOSFET transistor will be on during the time αT_h and blocked during the time (1-α) T_h. If p is the number of cycles during which the clock signal is applied to the transistor and q the number of cycles during which the clock signal is absent as shown in figure3, the switching frequency f_c of the MOSFET can be expressed by the relation [8],[9]:

$$f_c = \frac{p}{p+q} f_h \qquad (1)$$

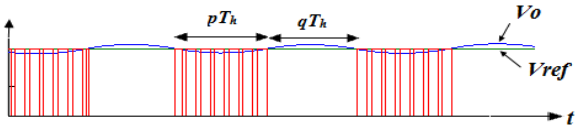


Figure-3. Evolution of Vo and the PSM control signal in steady state

The modulation factor M is defined by the relation:

$$M = \frac{q}{p+q} = 1 - \frac{f_c}{f_h} \qquad (2) \quad (0 \leq M \leq 1)$$

It is shown that in the case of the continuous conduction regime (CCM), the mean value of the voltage Vo applied to the resistor R_L is given by:

$$V_o = (1 - M)\alpha V_e \qquad (3)$$

α is the duty cycle of the clock signal.

From the relation (6), the average current Io circulating through RL is deduced:

$$I_o = \frac{V_o}{R_L} = (1 - M)\alpha V_e / R_L \quad (4)$$

It can be seen that only the modulation factor M can vary since the other parameters are constant. It is this variation which makes it possible to adjust the output voltage (Vo) to the reference voltage (Vref). It is also established that to remain in the continuous conduction mode (CCM), the load resistor R_L must satisfy the condition:

$$R_L \leq \frac{2Lf_h}{1-\alpha} \quad (5)$$

For a given load R_L , the inductance L must satisfy the condition:

$$L \geq \frac{R_L}{2f_h}(1-\alpha) \quad (6)$$

In our simulation, we considered the load R_L varies between 2 Ω and 50Ω, α = 0.9 and f_h = 100 kHz, Ve = 12V and C = 100µF.

From the relation (6), the minimum value of L is deduced:

$$L_{min} = 25\mu H$$

In the simulation we choose L = 200µH.

III. SIMULATION OF BUCK CONVERTER AND CONTROL FUNCTION UNDER ISIS

A. The hardware PSM control

The PSM function can be performed using a logic circuit as shown in the figure-3. When Vref > Vo, the output of the comparator (Compare to Zero) passes to 1 (D = 1, D input of the D Latch), the output Q of the D Latch passes to 1 and the output of the AND gate will reproduce the clock signal. When Vref < Vo, the input D of the D Latch passes to zero and subsequently the output Q, which will result in the blocking of the clock signal (output of the AND gate goes to zero).

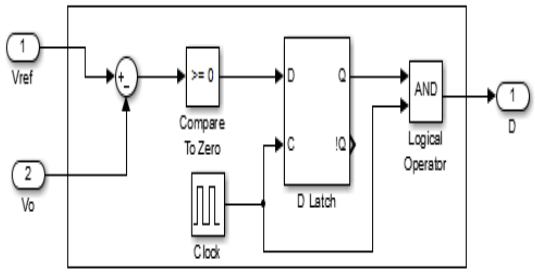


Figure-3. PSM circuit with logic gates

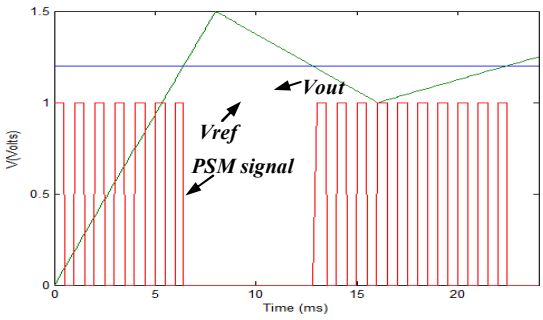


Figure-4. Evolution of PSM signal

Figure-4 Shows the evolution of the PSM signal. When Vo < Vref the clock signal is applied to the output of the circuit and when Vo > Vref the clock signal is blocked.

B. Complete circuit of hardware control under ISIS

The circuit representing the converter and the control part (figure-5) is carried out using the ISIS/Proteus software.

The control of the MOSFET RF470 used in this simulation will be provided by the driver IR2112. The pulse generator (CLK) supplies a rectangular signal at a frequency f_h = 100khz and with a duty cycle α = 0.9. The voltage dividers by means of high-value resistors serve to divide the reference voltage (Vref) and the output voltage (Vo) in the same proportions so that they do not exceed 5V, the maximum voltage accepted by the inputs of the comparator biased at 5V and the analog-to-digital converter input of the dsPIC (figure-10). The influence of these resistances is negligible for values of R_L not exceeding 100Ω.

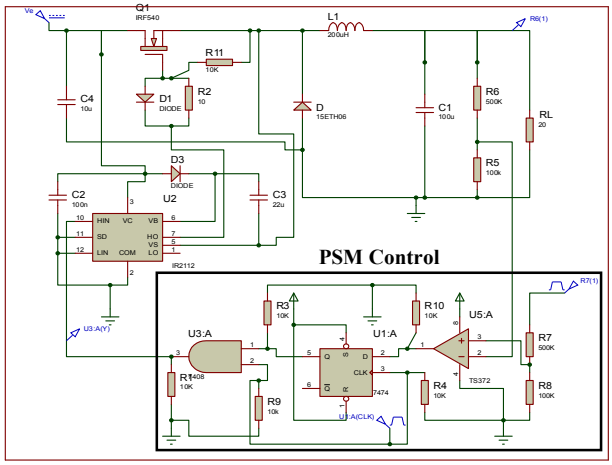


Figure-5. Converter and PSM circuit under ISIS

C. The software PSM control

The operating principle of the PSM control is summarized in the flow chart as shown in figure-6.

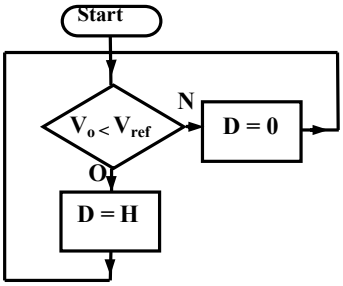


Figure-6. PSM function flow chart

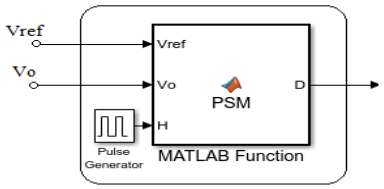


Figure-7. PSM Function

The PSM function which translates the flowchart of figure-6 is introduced in the form of a MATLAB function D = f (Vref, Vo, H) whose inputs are the reference voltage (Vref), the output voltage (Vo) The clock signal (H) [10]. Output D will send the clock signal H (figure-7) to the converter as long as Vo < Vref and block it when Vo > Vref. The advantage of this software solution with respect to a hardware implantation is the simplification of the control circuit. A single microcontroller containing the control program is sufficient instead of a circuit comprising several logic gates and a clock circuit [11].

D. Implementation of the control program in a dspic33 under MPLAB simulink blockset

The control part will be managed by a dsPIC33 according to the diagram in figure-8. The control in PSM mode will be implemented in a dsPIC33 microcontroller (16 bits) belonging to the Microchip family whose external clock frequency can reach 70MHz. The voltages Vo and Vref are applied to two inputs of the analog-to-digital converter integrated in the microcontroller and the output signal PSM is sent to a pin configured at the output as indicated in figure-9 and will be applied subsequently to the gate of the MOSFET through a driver [12], [13].

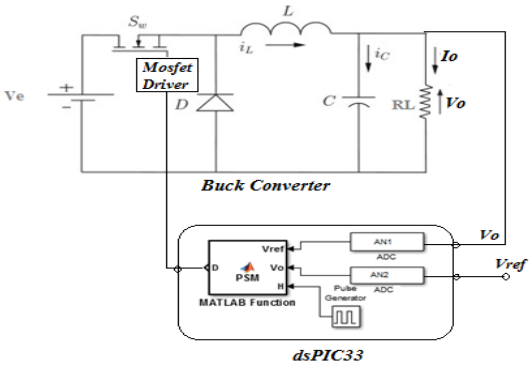


Figure-8. Buck converter and control circuit

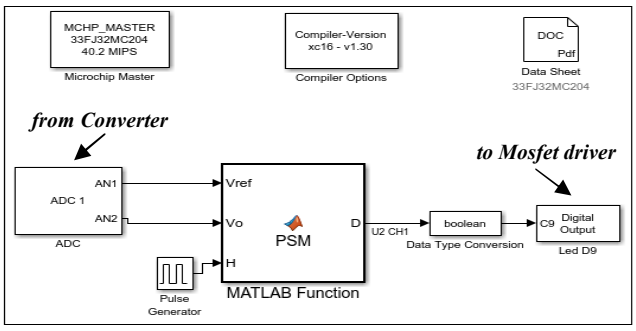


Figure-9. PSM function under MPLAB SIMULINK Blockset

Pulse generator supplies a rectangular signal at a frequency fh = 100khz and with a duty cycle α = 0.9 as in the previous case. The implementation of the PSM function is performed under version 3.39 of MPLAB Blockset for SIMULINK installed in the SIMULINK tool of MATLAB2016b software used in this study. In our simulation, we used the dsPIC33FJ32MC204. This microcontroller belongs to the microchip dsPIC family, performing very well with computing power which can reach 70 MIPS (70 million instructions per second) and simulable under ISIS/Proteus software. The compilation of the file under MPLABX interface using the xc16-v1.3 compiler will generate a source file in C language and the corresponding object file. It is the object file who will be charged in the program memoire of the dsPIC.

E. Complete circuit of software control under ISIS

The circuit representing the converter and the control part (figure-10) is carried out using the ISIS software.

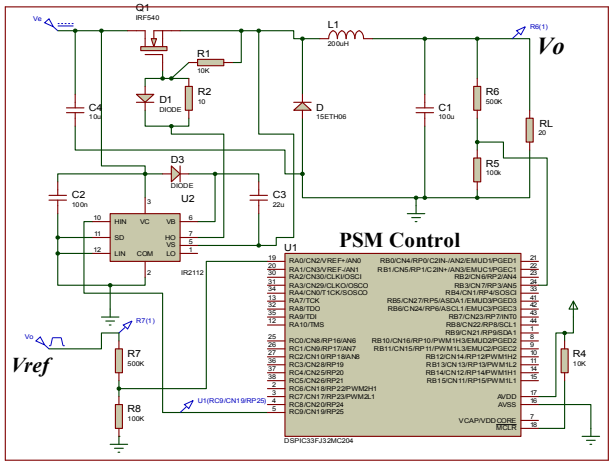


Figure-10. Converter and dsPIC controller under ISIS

IV. SIMULATION RESULTS AND DISCUSSION

A. Output voltage Vo and PSM signal evolution

The ISIS simulation of the converter response to a voltage step of 5,5V and delayed by 1 millisecond is given in figure-11. We note the appearance of a transitional phase before the establishment of the steady state.

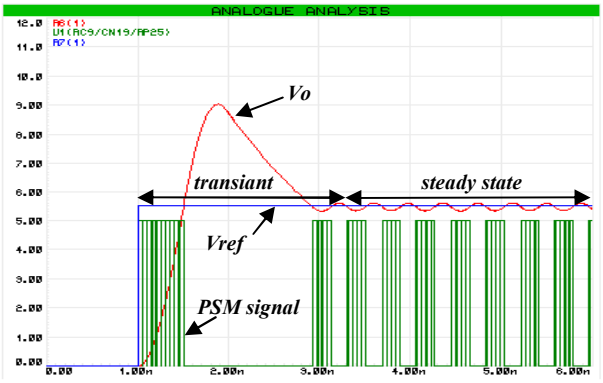
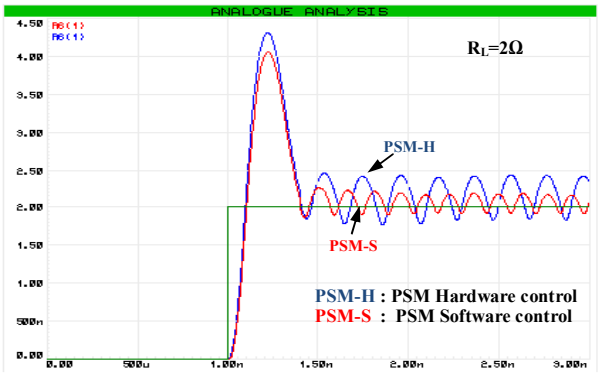


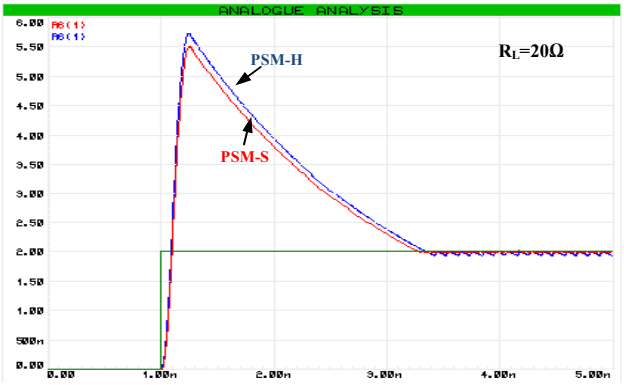
Figure-11. Output voltage Vo and PSM signal under ISIS

B. Evolution of Vo under the software and the hardware control at Vref = 2V for 3 values of R_L

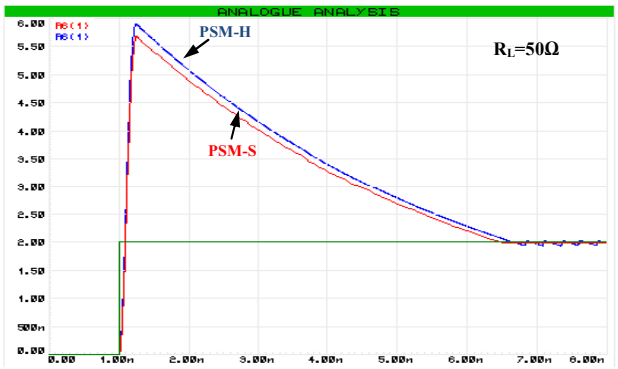
The figures12 (a), (b) and (c) shows the evolution of the output signal Vo corresponding to a reference voltage Vref = 2V and for different load resistances R_L. Note that for a small R_L value (R_L = 2Ω), the ripple is larger than for the high R_L values. However, it is noted that the ripple generated by the programmed PSM control is lower than in the case of the PSM cabled control. It is also noted that the response time of the converter increases when the value of R_L increases. When looking at the ripple more closely (case of Vref = 2V), it is noted that for R_L = 2Ω, the ripple in steady state generated by the programmed PSM control is of the order of 0.25Vpp, while the ripple due to the hardware PSM control is of the order of 0.6Vpp (figure-13) with a ratio of 0.42 .



(a)



(b)



(c)

Figure-12. Evolution of Vo versus time for 3 different values of R_L at V_{ref} = 2V

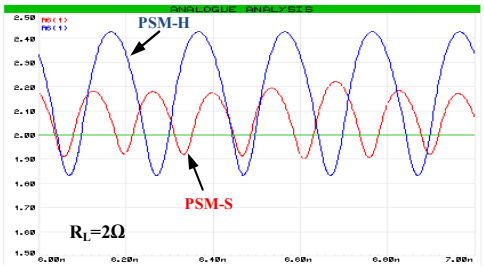
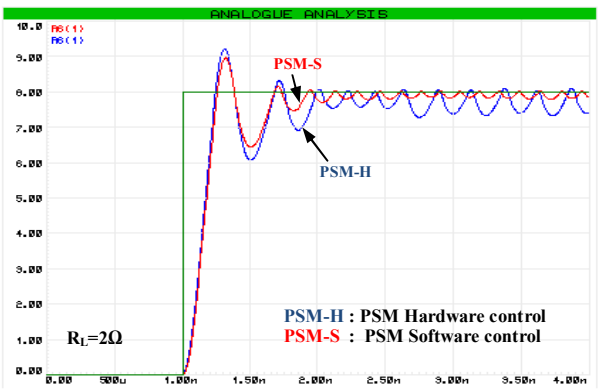


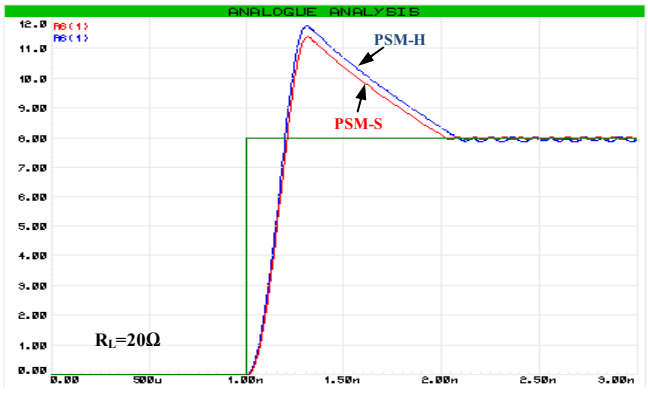
Figure-13 Ripple at steady state for R_L=2Ω and Vref=2V

C. Evolution of Vo under the software and the hardware control at Vref = 8V for 3 values of R_L

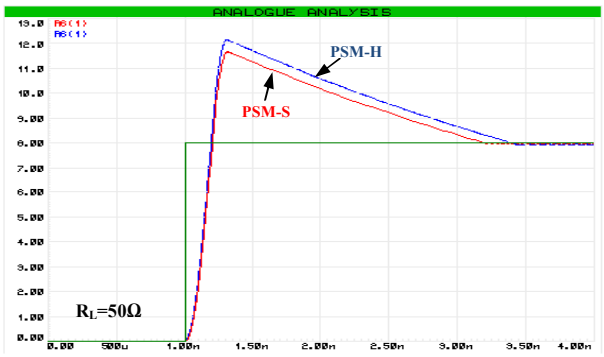
For a larger Vref value (Vref = 8V), it is noted that the ripple is always larger for the low values of R_L, as shown in the figures14 (a), (b) and (c) but for the same value of R_L the ripple due to PSM programmable control is lower than that generated by the hardware PSM control as in the previous case.



(a)



(b)



(c)

Figure-14. Evolution of Vo versus time for 3 different values of R_L at V_{ref} = 8V

The response time evolution versus R_L is comparable to the previous case. (the response time of the converter increases with R_L increases). On the other hand, the peak voltage of the transient phase is less accentuated than in the case where Vref = 2V for the three values of R_L. For R_L = 50Ω, the ripple under steady state generated by the programmed PSM control is of the order of 0.02Vpp, while the ripple due to the hardware PSM control is of the order of 0.08Vpp (figure-15) with a ratio of 0.25 . The decrease of the ripple for the large R_L values is a characteristic of the PSM mode control [14].

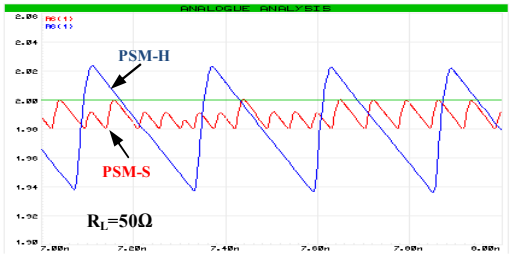


Figure-15. Ripple at steady state for R_L=50Ω and Vref=2V

D. Ripple ratios versus Vref

Figures 16 et 17 shows the ripple ratio (τ_{ond}) of Vo for different values of Vref for R_L = 2Ω and for R_L = 50Ω. It should be noted that in all cases the ripple rate generated by the programmed PSM control in steady state is always lower than the ripple rate of the hardware PSM control. It is also observed that in both cases (R_L = 2Ω and R_L = 50Ω) the ripple rate decreases when Vref increases.

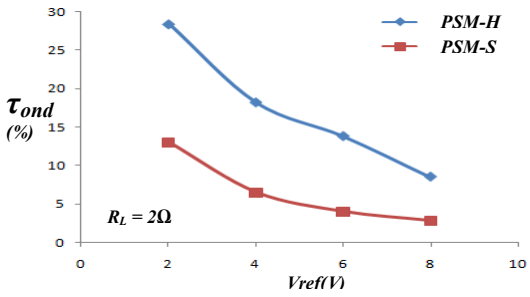


Figure-16. Ripple ratio of Vo versus V_{ref} at R_L=2Ω

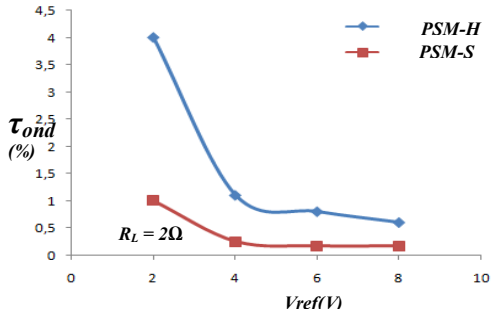


Figure-17. Ripple ratio of Vo versus V_{ref} at R_L=50Ω

V. CONCLUSION

In this study we studied the behavior of a Buck converter controlled in PSM (Pulse Skipping Modulation) mode, the control of which was introduced in two different ways. The first type of control is based on an electrical circuit based on conventional electronic components. The second type of control was introduced as a programmable control implemented on a microcontroller dspic . The advantage of this type of control is simplicity and flexibility, contrary to a conventional control. Thus, for example, the clock frequency can be modified by programming without changing any components.

The other advantage is the economics of the components, so a simple microcontroller can replace all the electrical circuit of the PSM control realized with a clock circuit and several logic gates. In order to program the PSM function, we used the MPLAB Blockset for SIMULINK tool, a powerful tool that allows to directly translating the schema of a circuit realized under SIMULINK into a program C, which will be compiled and loaded on a dsPIC. The use of this tool greatly and efficiently simplifies the graphical realization under SIMULINK contrary to the conventional methods. The comparison of the simulation results from the two methods shows that in addition to the advantages cited above, the programmed control has given better results, especially in terms of the decrease of the ripples in the steady state. The presence of ripples is the main defect of the PSM control.

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