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Analysis and Optimization of Dual Tail Comparator

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Abstract— To implement power efficient and high performance analog-to-digital converters the designers are urged to design an optimized dual tail comparator. In this paper, an analysis on the latency of the dual tail comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an insight about the main contributors to the comparator latency. Based on the presented analysis, a new dual tail comparator is proposed, where the circuit of a conventional dual tail comparator is modified to achieve power efficiency with high performance. It is shown that in the proposed dual tail comparator both the power and delay time is significantly reduced.

Keywords— Dual tail comparator, high-speed analog-to-digital converters (ADCs), low-power design.

1. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low-power comparators with small chip area. High-speed comparators in ultra deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low-voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs. Many techniques, such as supply boosting methods [2], [3], techniques employing body-driven transistors [4], [5], current-mode design [6] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock [4], removes the threshold voltage requirement such that body-driven MOSFET operates as a depletion-type device. Based on this approach, in [5], a 1-bit quantizer for sub-1V __ modulators is proposed. Despite the advantages, the body-driven transistor suffers from smaller transconductance (equal to g_{mb} of the transistor) compared to its gate-driven counter-part while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration. Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In [7]–[9], additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of [7] works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μ W. Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of dual tail dynamic comparator first proposed in [10] is based on designing a separate input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range [10].

In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architec-tures. Furthermore, based on the dual tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few minimum-size transistors to the conventional dual tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in con-siderable power savings when compared to the conventional dynamic comparator and dual tail comparator.

2. CLOCKED REGENERATIVE COMPARATORS

Clocked regenerative comparators have found wide appli-cations in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common struc-tures, i.e., conventional dynamic comparator and conventional dynamic dual tail comparator are analyzed, based on which the proposed comparator will be presented.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic com-parator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and M_{tail} is off, reset transistors (M_7–M_8) pull both output nodes Out*n* and Out *p* to V_{DD} to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = V_{DD}, transistors M_7 and M_8 are off, and M_{tail} is on. Output voltages (Out *p*, Out*n*), which had been pre-charged to V_{DD}, start to discharge with different discharging rates depending on the corresponding input volt-age (INN/INP). Assuming the case where $V_{INP} > V_{INN}$, Out *p* discharges faster than Out*n*, hence when Out *p* (discharged by transistor M_2 drain current), falls down to V_{DD}–$|V_{thp}|$ before Out*n* (discharged by transistor M_1 drain current), the Fig. 2. Schematic diagram of the conventional dual tail dynamic com-parator corresponding pMOS transistor (M_5) will turn on initiating the latch regeneration caused by back-to-back inverters (M_3, M_5 and M_4, M_6). Thus, Out*n* pulls to V_{DD} and Out *p* discharges to ground. If $V_{INP} < V_{INN}$, the circuits works vice versa.

B. Conventional Dual tail Dynamic Comparator

A conventional dual tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider M_{tail2}, for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset [10].

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, M_{tail1}, and M_{tail2} are off), transistors M_3-M_4 pre-charge fn and fp nodes to V_{DD}, which in turn causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), M_3-M_4 turn off and volt-ages at nodes fn and fp start to drop with the rate defined by $I_{Mtail1}/C_{fn\ (p)}$ and on top of this, an input-dependent differential voltage $\_V_{fn(p)}$ will build up. The intermediate stage formed by M_{R1} and M_{R2} passes $\_V_{fn(p)}$ to the cross-coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

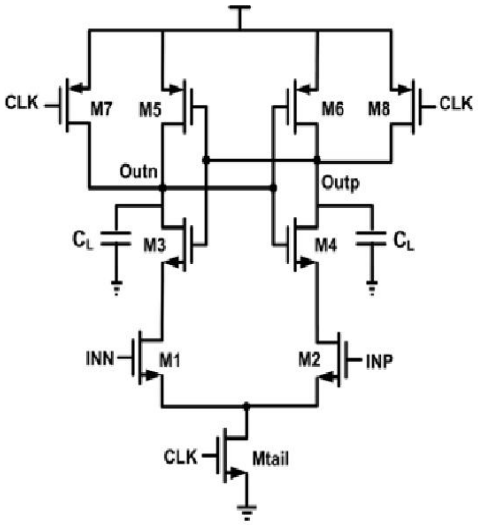

Fig. 1. Schematic diagram of the conventional dynamic comparator

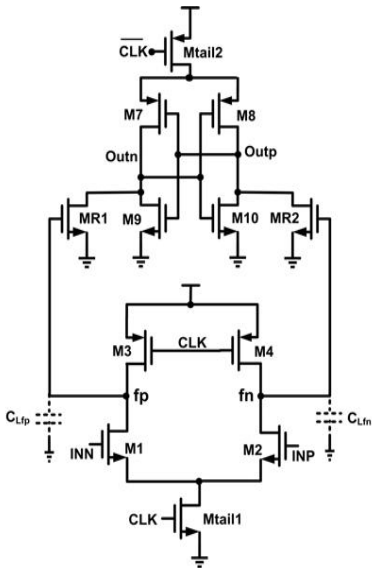

Fig. 2. Schematic diagram of the conventional dual tail dynamic comparator

3. PROPOSED DUAL TAIL DYNAMIC COMPARATOR

Fig. 5 demonstrates the schematic diagram of the proposed dynamic dual tail comparator. Due to the better performance of dual tail architecture in low-voltage applications, the proposed comparator is designed based on the dual tail structure. The main idea of the proposed comparator is to increase $\_V_{fn/fp}$ in order to increase the latch regeneration speed. For this purpose, two control transistors (M_{c1} and M_{c2}) have been added to the first stage in parallel to M_3/M_4 transistors but in a cross-coupled manner [Fig. 3].

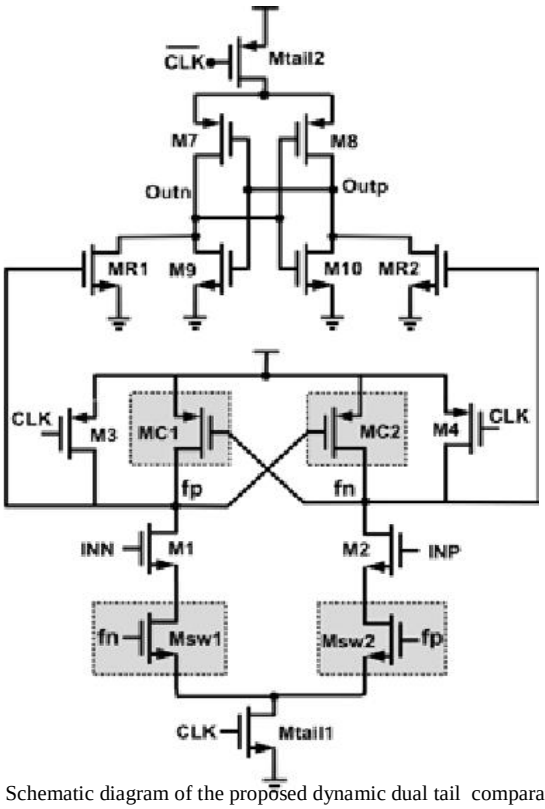

Fig.3. Schematic diagram of the proposed dynamic dual tail comparator

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both fn and fp nodes to V_{DD}, hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2}, reset both latch outputs to ground.

During decision-making phase (CLK = V_{DD}, M_{tail1}, and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about V_{DD}). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus fn drops faster than fp, (since M_2 provides more current than M_1). As long as fn continues falling, the corresponding pMOS control transistor (M_{c1} in this case) starts to turn on, pulling fp node back to the V_{DD}; so another control transistor (M_{c2}) remains off, allowing fn to be discharged completely. In other words, unlike conventional dual tail dynamic comparator, in which $\_V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference (9), in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (M_{c1}) turns on, pulling the other node fp back to the V_{DD}. Therefore by the time passing, the difference between fn and fp ($\_V_{fn/\ fp}$) increases in an exponential manner, leading to the reduction of latch regeneration time (this will be shown in Section III-B). Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., M_{c1}) turns on, a current from V_{DD} is drawn to the ground via input and tail transistor (e.g., M_{c1}, M 1, and M_{tail1}), resulting in static power consumption.

4. SIMULATION RESULTS

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all cir-cuits have been simulated

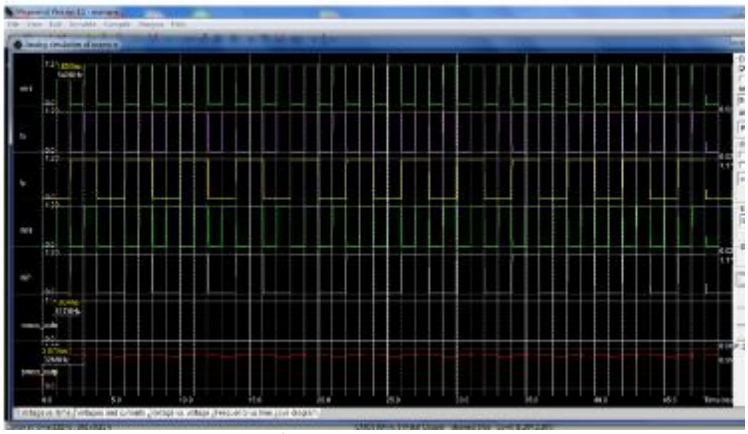

Fig.4. Simulation result of conventional dynamic dual tail comparator

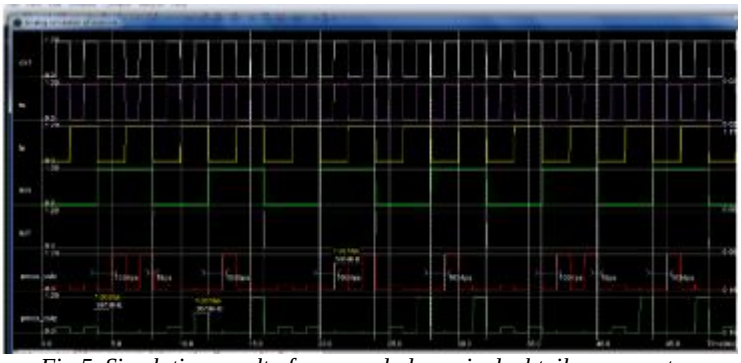

Fig.5. Simulation result of proposed dynamic dual tail comparator

The power waveforms of conventional dual tail comparator is compared with proposed comparator. The waveforms are shown below.

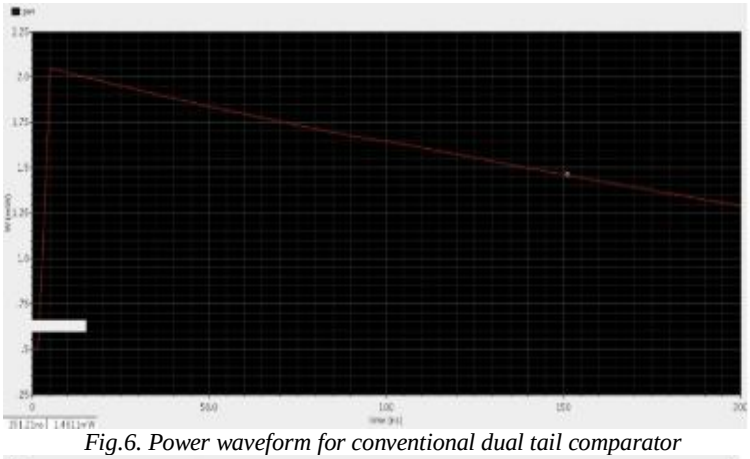

Fig.6. Power waveform for conventional dual tail comparator

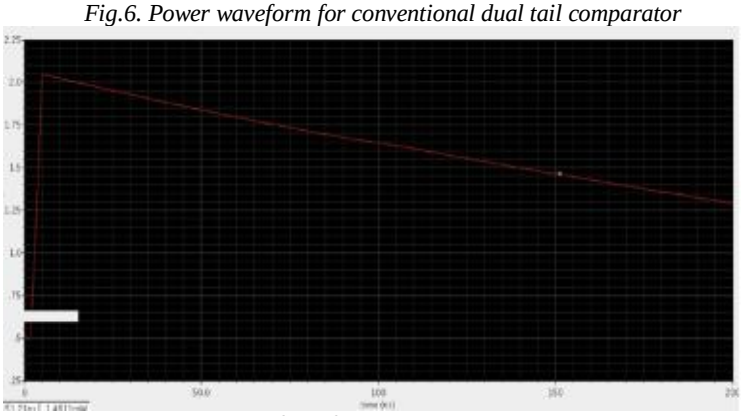

Fig.7. Power waveform for proposed dual tail comparator

The above waveforms, shows that proposed comparator consumes less power than the conventional one.

5. Conclusion

In this paper, we presented a analysis of dual tail comparator in terms of power, area and delay. Two common structures of conventional dynamic comparator and conventional dual tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with LVLP capability was proposed in order to improve the performance of the comparator.

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