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FinDET Based Power and Delay Optimized Computational Unit for Medical Image Compression

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Abstract: High-performance computational units are critical in medical imaging applications where real-time processing and low power consumption are essential. Medical image compression requires efficient hardware architectures capable of handling massive data volumes without compromising diagnostic quality. This paper presents a power- and delay-optimized computational unit based on FinFET Double- Edge Triggered (FinDET) flip-flops. By combining the superior electrostatic control of FinFET technology with the dual-edge triggering mechanism, the proposed architecture reduces clock frequency requirements while maintaining high throughput. Simulation results demonstrate that the FinDET architecture significantly improves the Power-Delay Product (PDP) compared with conventional CMOS designs. The proposed unit is optimized for medical image compression algorithms such as Discrete Wavelet Transform (DWT) and Discrete Cosine Transform (DCT), making it suitable for portable diagnostic devices and high-speed clinical imaging systems.
Keywords: FinFET, Double Edge Triggered (DET), Medical Image Compression, Power Optimization, Delay Optimization, Computational Unit, VLSI Design.

I. INTRODUCTION

The rapid evolution of digital healthcare has led to an exponential increase in the demand for high-resolution medical imaging technologies such as Magnetic Resonance Imaging (MRI), Computed Tomography (CT), and ultra sound systems. These imaging modalities generate large volumes of data, making efficient image compression necessary to reduce storage requirements and transmission bandwidth. Traditional computational units designed using conventional CMOS technology face challenges such as increased leakage current and higher power dissipation as device scaling approaches the nanometer regime. These issues significantly affect portable medical devices where energy efficiency and thermal constraints are critical. To address these challenges, this work proposes a FinFET-based computational unit using Double-Edge Triggered (DET) flip-flops, referred to as the FinDET architecture. Unlike Single-Edge Triggered (SET) flip-flops, which operate only on the rising or falling edge of the clock signal, DET flip-flops capture data on both edges of the clock. This enables the system to operate at half the clock frequency while maintaining the same data throughput, resulting in reduced dynamic power consumption.

II.LITERATURE SURVEY

Recent developments in semiconductor technology have led to the transition from planar MOSFET devices to three-dimensional FinFET structures. FinFET devices provide improved gate control over the channel, effectively reducing short-channel effects and leakage currents in deeply scaled technologies. Several studies on medical imaging hardware indicate that compression algorithms require significant computational resources, leading to latency and power consumption challenges. Hardware acceleration has therefore become essential for real-time imaging systems. Previous research on Double-Edge Triggered (DET) flip-flops demonstrates their effectiveness in reducing clock frequency requirements and dynamic power consumption in digital signal processing applications.

III. PROPOSED SYSTEM

A. FinDET Architecture

The proposed computational unitutilizes FinFET transistors arranged in a Double-Edge Triggered flip-flop architecture.
Key Features:

- Clocking Mechanism – DET flip-flop captures input data during both the rising and falling edges of the clock signal.
- Power Efficiency – Clock frequency can be reduced by approximately 50%, lowering dynamic power consumption.
- Delay Optimization – FinFET technology offers faster switching and reduced critical path delay.

B. System Block Diagram

Input Medical Image Data → FinDET Based Transform Unit (DCT/DWT) → Quantization Module → Entropy Coding → Compressed Image Output

IV. SYSTEM REQUIREMENTS

C. Functional Requirements

- Dual-Edge Processing
- Compression Accuracy
- Operational Stability

D. Non-Functional Requirements

- Response Time
- Power Efficiency
- Scalability

V.RESULTS AND DISCUSSION

The proposed FinDET computational unit was simulated using Electronic Design Automation (EDA) tools such as Cadence Virtuoso and HSPICE at advanced FinFET technology nodes (e.g.,14nm or 7nm).

Power Analysis: DET clocking reduces clock network power consumption. Delay Analysis: FinFET devices reduce propagation delay.

Image Quality Evaluation: PSNR remains within acceptable medical imaging standards when tested with DICOM datasets.

VI. CONCLUSION

This paper presents a FinFET-based Double- Edge Triggered computational unit (FinDET) designed for medical image compression applications. The combination of FinFET leakage control and DET clock efficiency improves power efficiency and reduces delay. Simulation results show improved Power-Delay Product (PDP) compared with conventional CMOS-based SET designs. The architecture is suitable for portable diagnostic devices and high speed imaging systems. Future work includes integrating the FinDET computational unit into a complete System-on- Chip (SoC) architecture for wearable medical monitoring systems and AI-assisted diagnostic platforms.

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