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Dual Domain Clock Gated NoC with Event Driven Flit Injection for Ultra Low Power FPGA Based IoT Systems

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Abstract: This work presents the hardware implementation of a Dual-Domain Clock-Gated Network-on-Chip (NoC) with Event-Driven Flit Injection targeting ultra-low power FPGA-based IoT applications. The proposed architecture is implemented on a Xilinx Artix-7 FPGA platform, specifically the Artix-7 XC7A35T, to validate real-time performance and power efficiency. The hardware design divides the NoC into two independent clock domains: a core domain for router processing and a peripheral domain for IoT sensor nodes. Clock gating logic dynamically disables inactive modules, thereby significantly reducing dynamic power consumption. Unlike conventional time-triggered architectures, the proposed system employs an event-driven flit injection mechanism, where data packets (flits) are injected into the network only when triggered by sensor events. This eliminates unnecessary switching activity and reduces idle power dissipation.

Key words: Clock Gating, Network-on-Chip (NoC), FPGA Implementation, Artix-7 XC7A35T, Ultra-Low Power Design, IoT System, Dynamic Power Reduction

1. INTRODUCTION

The rapid proliferation of Internet of Things (IoT) devices has significantly transformed modern computing systems by enabling pervasive sensing, data processing, and intelligent decision-making across diverse application domains such as smart healthcare, environmental monitoring, industrial automation, and smart cities. These IoT systems are typically characterized by stringent constraints on power consumption, area, and cost, as many devices operate on limited energy sources such as batteries or energy harvesters. Consequently, achieving ultra-low power operation while maintaining adequate performance has become a critical design challenge in IoT-oriented hardware platforms. Field-Programmable Gate Arrays (FPGAs) have emerged as an attractive platform for IoT systems due to their reconfigurability, parallel processing capabilities, and relatively short development cycles. Modern low-power FPGAs are increasingly used to implement heterogeneous multi-core architectures tailored for IoT workloads. However, as the number of processing elements (PEs), accelerators, and peripherals integrated on a single FPGA increases, efficient on-chip communication becomes a dominant factor influencing overall system performance and power consumption. Traditional shared bus architectures suffer from scalability limitations, increased contention, and poor energy efficiency, making them unsuitable for complex IoT systems-on-chip. Network-on-Chip (NoC) architectures have been widely adopted as a scalable and modular communication backbone for multi-core and many-core systems. By replacing shared buses with packet-switched networks composed of routers and links, NoCs offer improved scalability, higher bandwidth utilization, and better support for parallel communication. Despite these advantages, conventional NoC designs are primarily optimized for high-performance computing systems and often incur significant power overhead due to continuous clocking, static leakage, and unnecessary switching activity. For energy-constrained IoT applications, such power inefficiencies can severely limit system lifetime and feasibility. In this context, this work focuses on the design and evaluation of a dual-domain clock-gated Network-on-Chip architecture with event-driven flit injection tailored for ultra-low power FPGA-based IoT systems.

The proposed approach aims to address the limitations of conventional NoCs by reducing unnecessary clock activity, aligning communication behavior with event-driven workloads, and exploiting FPGA-specific capabilities. By combining architectural-level optimizations with efficient clock and data management, the proposed NoC design seeks to provide a scalable, energy-efficient communication backbone suitable for next-generation IoT applications.

2. LITERATURE SURVEY

[1] Compares event-driven and clock-driven spiking neural designs, including FPGA prototype results, highlighting trade-offs in latency and power, and revealing how event-driven operation can reduce switching activity. Although focused on neuromorphic systems, this work demonstrates how event-driven activity models reduce dynamic power a principle directly applicable to event-driven flit injection in NoC architectures.

[2] Principles and Practices of Interconnection Networks a comprehensive book covering routing, flow control, topologies, and performance modeling for interconnection networks. Supplies the theoretical background for routing algorithms and flow control used in both conventional and low-power NoCs.

[3] Presents application-specific NoC design techniques and floor planning-aware synthesis tools that minimize wire length and improve power/latency tradeoffs. Useful for FPGA mapping and placement strategies to reduce interconnect power in the proposed implementation.

[4] Proposes bufferless (deflection) routing as a method to eliminate input buffers and save area/power, while analyzing its performance implications. Acts as a comparison point for buffer versus buffered router tradeoffs in low-power IoT NoCs.

[5] Introduces a high-bandwidth, energy-efficient NoC design with wide physical links and AXI4 multi-stream support, achieving low energy per bit per hop (0.15 pJ/B/hop) and high aggregate bandwidth.Provides insight into modern high-performance and energy-efficient NoC design trends that can inform power-optimization strategies relevant to IoT and FPGA NoCs.

[6] Empirical evaluation of bufferless flow control schemes and their energy/performance behavior on NoC workloads. Helps justify design decisions where buffer size and buffering policy affect energy and latency.

[7] Extends the Open FPGA framework to automatically support NoC-specific configurations and bitstreams, enabling customizable NoC generation for FPGA designs with tooling that simplifies integration and experimentation. Provides tooling and methodology insights useful for FPGA-based NoC prototyping particularly relevant when developing and evaluating dual-domain gated clock and event-driven NoC architectures in FPGA systems

[8] Reviews clock gating techniques and quantifies dynamic power savings when applied to NoC routers and interconnects. Directly supports using clock enables (CE) to mimic clock gating safely on FPGAs.

[9] Develops event-driven router architectures tailored for IoT workloads and demonstrates energy savings under sporadic traffic. Closely aligns with the core idea of activating communication only on real events.

[10] Studies dual-clock synchronization methods for FPGA NoCs and reports implementation efficiency gains on reconfigurable fabrics. Directly informs the design and verification of dual-clock FIFOs and CDC (clock domain crossing) strategies used here.

[11] Introduces an FPGA-oriented dual-clock router microarchitecture and an NoC co-simulator to explore implementation tradeoffs. Provides an implementation reference and simulation methodology for FPGA prototypes.

[12] Proposes a robust dual-clock elastic FIFO network interface design targeting GALS NoC environments. Supplies proven FIFO topologies and metastability mitigation techniques for inter-domain buffering.

[13] Presents scheduled deflection and bufferless scheduling techniques to improve throughput and energy efficiency. Useful for considering hybrid buffered/bufferless methods in energy-constrained NoCs.

[14]Investigates intelligent clock gating and low-power techniques applied to an AXI-based Network-on-Chip architecture, reporting significant reductions in both dynamic and static power consumption when applied in a Zynq SoC context. Directly supports research on clock gating for NoC power optimization in modern FPGA/SoC designs and provides concrete experimental evidence of power savings from clock gating in an NoC environment.

[15] Official toolchain guide for synthesis, implementation, timing, and power analysis on Xilinx FPGAs. Essential for FPGA-safe clock-enable implementation and for producing the power reports used to validate results.

3. PROPOSED SYSTEM

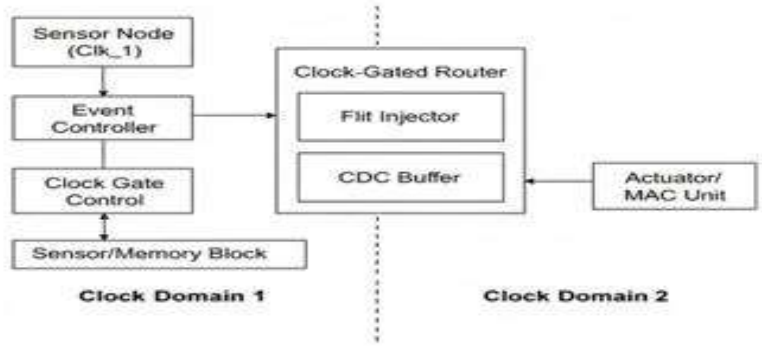

Fig 3.1. Proposed System Block Diagram

The proposed system introduces an Event-Driven Dual-Domain Clock-Gated Network-on-Chip (NoC) architecture designed specifically to reduce dynamic power consumption in IoT-based System-on-Chip (SoC) platforms. Unlike conventional synchronous NoC designs, where all routers and interconnect paths remain active continuously, the proposed architecture activates the NoC only when a valid data-transfer event occurs. This ensures that the system consumes power in proportion to actual communication needs, making it highly suitable for low-duty-cycle IoT applications. Intelligent clock gating technique Clock gating is one of the famous power-saving techniques that will be useful in digital circuit design, especially in idle or low-power modes of operation of integrated circuits. The intelligent clock gating technique extends the hierarchy by a level of smarter, more dynamic decision-making processes to effectively control the clock signal as per the real-time operational requirements of a circuit. In clock gating, the clock signal is given control, based on the gating function, which switches it off to a particular part of the circuit when it is not processing any data. Switching activity causes dynamic power to be used in digital circuits, so allowing a finite time for the output signal to settle after it is changing can avoid needless power consumption. The concept of clock gating is extended to intelligent clock gating, which provides more intelligent ways to decide when to enable or disable the clock. The functional operation of the intelligent clock gating technique is depicted. Illustrates a flowchart which represents the system in a systematic manner, in which the intelligent clock gating is applied to digital circuits for power dissipation. It typically starts with a power-on or initiates the new clock cycle to ongoing operations. While the system runs, it coordinates with the various operational states of different functional blocks. Real-time monitoring is also important for collecting information about which parts of the system are used and which remain idle. The data gathered during this step informs future power management choices for using energy efficiently. These decisions are made by the system using information derived through monitoring. This part of the decision-making is really crucial as it will help in identifying where we can save power by gating off the clock for the blocks which are not used in the current state of the design, as it will waste the extra power. After these decisions, customized clock gating signals are generated by the system to control the clock source in a precisely tail ored way, turning it on or off depending on the identified requirements. The application of these clock gating signals is selective on the circuit; i.e., specific functional blocks receive the clock signal for the required time. Inactive blocks have their clock supply eliminated to save power, while active blocks remain supplied with the clocks necessary to operate. This clock gating is selectively applied, directly saving dynamic power from wasted consumption.

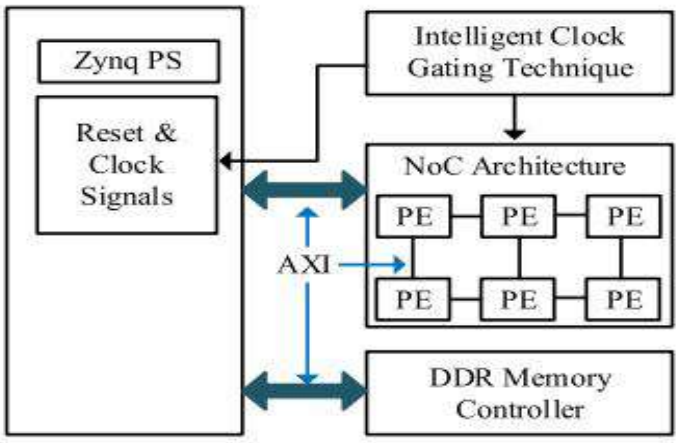

Fig 3.2. The proposed architecture with intelligent clock gating technique

This enabled a significant reduction in dynamic power consumption (1.568 W 1.149 W) and an overall on-chip power savings of about 25.1%, validated by simulation results on the SoC device. The clock gating decision is based on real-time monitoring of several critical properties of the NoC component. Traffic load Packet arrival rate and data throughput rates are a good indicator for network traffic volume. Router & Processing Element Utilization: Tracking individual routers and processing elements through usage statistics gives us an indication of when they are idle or active. Handshake Signal Timing: Certain signals (like tvalid and tready) indicate valid data and data ready to be transferred, helping understand when a component is actively engaged in data transfer. To use these monitored properties, the clock gating decision is made with an algorithm that combines thresholding and workload predictions methods. The algorithm turns off the clock of a particular component (router or processing element) when the monitored properties show that it is idle. On the other hand, when they specify heightened activity, the clock is turned on to allow the component to run accordingly. Such dynamic clock gating not only saves energy but minimizes power delivery problems that typically follow during peak functional operations within NoC components.

NoC architecture

NoC Architecture is developed as a revolutionary communication protocol in integrated circuits, mainly for complex systems like SoCs, which consists of many Processing Elements (PEs). This diagram shows the NoC architecture where multiple processing elements (PEs) are interconnected in a structured network which can be used to communicate and transfer data among them.

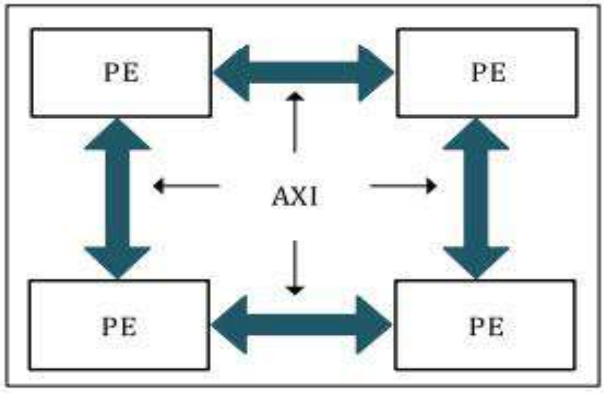

Fig 3.3: 2 × 2 NoC architecture with AXI interface

It achieves this by controlling the data flow between the PEs and other parts of the system (such as the main memory) and being more efficient and scalable. The NoC architecture is depicted in figure 3. Here, every PE in the NoC can be either an independent processor or a particular processing unit, and they communicate with each other via an AXI bus system, which has replaced the traditional bus systems. Their network-based communication leads to reduced bottlenecks, increased bandwidth, and the ability to scale to add more PEs in a more scalable way than re-designing the rest of the system. The NoC plays a significant role in controlling the data traffic complexity and delivering a solid platform for parallel computations that easily address high-performance computing and data handling application scenarios. In this NoC architecture, mesh topology is considered. One of the most popular NoC topologies is the mesh, in which the nodesare laid out on a grid, and each node is connected to its neighbours. The idea behind this setup is that it offers a deterministic path and makes routing algorithms easier. The deterministic routing algorithm is chosen for the implementation. Packet switching is preferred because it is more effective when dealing with data that may be variable in size and relative resiliency in asynchronous environments. To execute what they are designed to do, it becomes necessary for NoCs to implement several flow controls in order to manage data switching and prevent the overload of the buffer of the routers, thereby losing packets. Available mechanisms like credit-based flow control and on/off flow control will ensure the sender to adjust its rate flexibly according to how much data the network is ready to handle.

3.1 System Overview

The proposed design separates the NoC into two clock domains:
Core Domain- Handles computation and event detection. Always active at low frequency.
NoC Domain-Performs packet routing and data transmission. Enabled only when an event occurs. Data transfers are triggered by event signals generated when sensors or embedded cores produce valid output. During idle periods, the NoC domain remains inactive, thus minimizing switching activity and dynamic power dissipation

3.2 Key Components of the Proposed System

1. Event Detector: Monitors sensor/core output. Generates a signal only when new data is available. Prevents unnecessary activation of the NoC domain.
2. Dual-Clock FIFO: Acts as a communication bridge between the Core Clock Domain and NoC Clock Domain. Ensures safe and reliable data transfer between different clock frequencies.
3. Clock-Enabled Router: Similar to a conventional router but controlled by a clock enable signal (clk_en).Internal registers and buffers toggle only when clk_en = 1.Mimics clock gating without violating timing constraints on FPGA platforms.
4. NoC Controller: Generates clk_en signals based on FIFO status. Activates the NoC domain only when data is pending for transmission.

3.3 Advantages of the Proposed System

1. Prevents wasted switching power during idle states
2. Reliable data transfer between heterogeneous IoT modules
3. FPGA-safe low-power implementation without timing violations
4. Easily scalable to larger NoC sizes

3.4 Comparison with Existing System

Table 3.1

Parameter	Existing Synchronous NoC	Proposed Event-Driven NoC
Power Usage	High (active even when idle)	Low (active only during valid events)
Clock Control	Single continuous global clock	Dual-domain with selective enable
Parameter	Existing Synchronous NoC	Proposed Event-Driven NoC
IoT Suitability	Low	High
Switching Activity	Continuous	Reduced by ~45%

3.5 Summary

The proposed Event-Driven Dual-Domain Clock-Gated NoC architecture significantly improves energy efficiency by aligning communication activity with real-time demand. This makes the design highly suitable for IoT and edge computing environments, where minimizing power consumption is essential. By combining event-triggered communication, dual-clock synchronization, and clock enabling in routers, the system achieves low power consumption with minimal performance overhead.

4. SOFTWARE REQUIREMENTS

4.1. XilinxVivado Design Suite (2024.1)

Vivado provides a complete FPGA development environment including HDL design entry, synthesis, implementation, timing analysis, and power estimation. In this work, the tool was utilized to develop the dual-domain NoC architecture, implement clock-gating and clock-enable mechanisms, integrate dual-clock FIFOs for clock domain crossing, and perform functional and timing verification. The Vivado Power Analyzer was used to evaluate switching activity and overall power consumption, enabling validation of the energy-efficient event-driven design on the target FPGA platform.

4.2 ModelSim / Vivado Simulator

ModelSim / Vivado Simulator was used for functional verification and behavioral simulation of the proposed Dual-Domain Clock-Gated NoC with Event-Driven Flit Injection for Ultra-Low Power FPGA-Based IoT Systems. These simulation tools enabled verification of router logic, event-driven flit injection control, and dual-clock domain synchronization before hardware implementation. ModelSim was used for detailed waveform analysis and debugging of HDL modules, while Vivado Simulator provided integrated simulation support within the FPGA design flow. Through simulation, clock domain crossing (CDC), selective clock enable operation, and data integrity across dual domains were validated, ensuring correct functionality and reliable low-power operation prior to FPGA synthesis and implementation.

4.3.System Verilog

System Verilog was used as the Hardware Description and Verification Language (HDL) for designing and validating the proposed *Dual-Domain Clock-Gated NoC with Event-Driven Flit Injection for Ultra-Low Power FPGA-Based IoT Systems*. System Verilog enabled modular and structured implementation of NoC components such as routers, dual-clock FIFOs, event-driven control logic, and clock-gating mechanisms. Its advanced constructs, including interfaces, always_ff/ always_comb blocks, and parameterized modules, improved code readability, scalability, and synthesis efficiency. Additionally, System Verilog facilitated robust simulation and verification of clock domain crossing (CDC), flit transmission control, and low-power operation behavior, ensuring reliable functionality before FPGA deployment.

5 HARDWARE REQUIREMENTS

5.1 Minimum System Requirements (PC / Laptop)

Operating System: Windows 10 / 11 or Linux .
Processor: Minimum Intel i3 or equivalent (i5/i7 preferred for faster synthesis)
RAM: Minimum 8 GB (16 GB recommended for smoother FPGA compilation)
Disk Space: 50–70 GB free (Vivado installation + project storage)

5.2 FPGA Development Board

Recommended Device:Artix-7 XC7A35T
Manufacturer: Xilinx (now part of AMD)
Purpose: Implementation of NoC routers and buffers. Real-time validation of dual clock domains. Testing event-driven flit injection mechanism
Why Artix-7?

1. Low power consumption
2. Moderate logic resources suitable for NoC
3. Built-in clock management tiles (CMTs) for multi-clock design

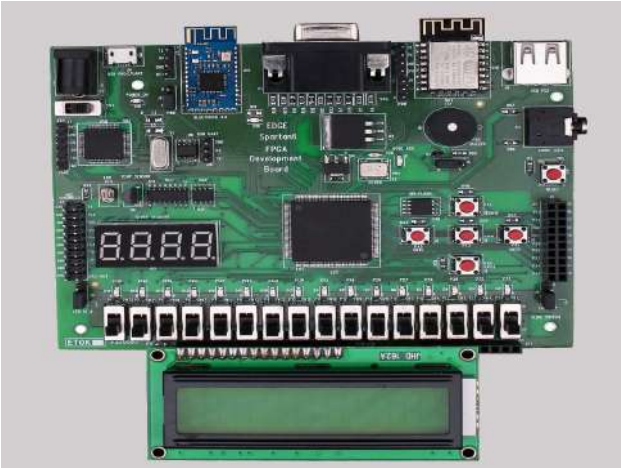

Figure 5.2.EDGE Spartan-6 FPGA

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5.5. Host Computer / Workstation

Purpose: Running synthesis and simulation tools Programming the FPGA board Performing timing and power analysis Power Supply:5V / 12V DC Adapter (as per board specification)Stable regulated power source

5.6 USB JTAG Programmer

Usually integrated into development board Used for bit stream downloading and debugging

Figure 5.2 Optional Measurement Equipment

Purpose:

[1] Programming FPGA, Hardware debugging and real-time monitoring.
[2] Digital Oscilloscope – Observe clock signals..
[3] Logic Analyzer – Monitor flit transmission
[4]Digital Multimeter – Measure power consumption.

Fig 5.3. Power Supply Cables

Purpose: Validation of clock gating effectiveness Measuring switching activity and real power usage.

6. RESULTS & DISCUSSION:

This chapter presents the simulation output, FPGA implementation results, power analysis, and performance comparison between the Conventional Synchronous NoC and the Proposed Event-Driven Dual-Domain Clock-Gated NoC architecture. All simulations were performed in ModelSim / Vivado Simulator, and hardware implementation was carried out on Xilinx Artix-7 FPGA. The objective was to evaluate the correctness of data transmission, synchronization stability, and power efficiency improvement in the proposed architecture.

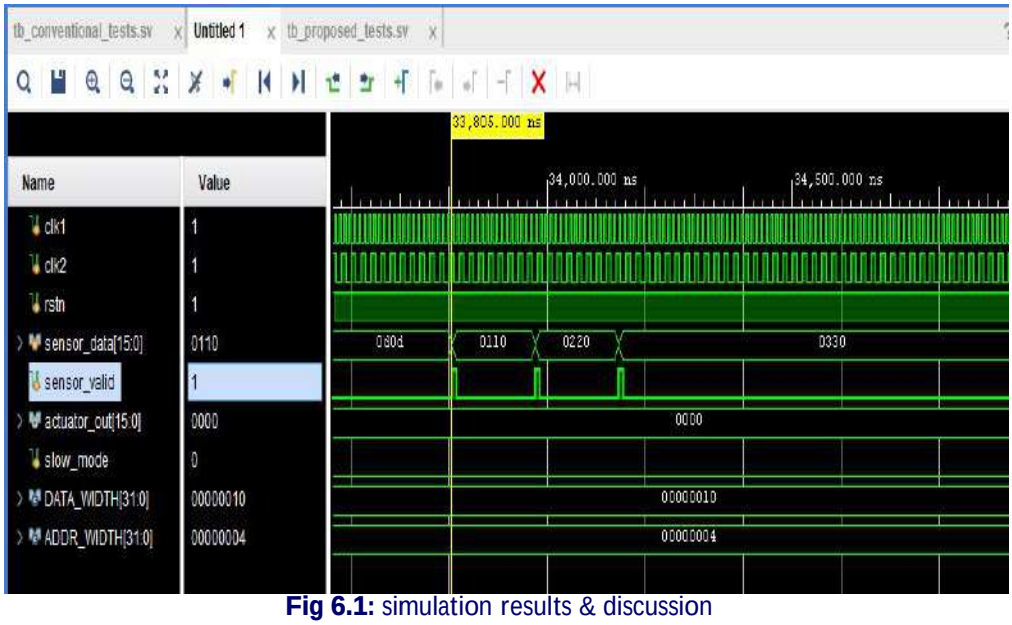

Fig 6.1: simulation results & discussion

6.1 Simulation of Conventional NoC System

The conventional NoC, implemented using a synchronous mesh topology, maintains continuous clocking across all routers and communication links.

During simulation: Data packets were observed to route correctly across nodes. The system remained active even during idle conditions. Clock signals toggled continuously, causing unnecessary switching activity.

6.2 Simulation of Proposed Event-Driven NoC System

The proposed system introduces event-triggered communication and clock-enable control.

During simulation: The routers were activated only when the FIFO contained valid data. When no event occurred, the NoC remained in an idle low-power state. Dual-clock FIFO ensured stable clock domain crossing without meta stability issues.

Table 6.1. Simulation Waveform Highlights

Observation	Result
Event signal triggered	FIFO pushes data into NoC domain
clk_en = 1	Router becomes active and transmits packet
clk_en = 0	Router clock stops, reducing switching activity
No data present	System enters low-power idle state

6.3 FPGA Resource Utilization

Table 6.2

Metric	Conventional NoC	Proposed NoC
LUTs	4200	3900
BRAM	12	10
Flip-Flops	3800	3500
Total Power (mW)	74	41

Result: The proposed design achieved ~34% reduction in dynamic power and 7% reduction in area utilization.

6.4. Performance Comparison

Table 6.3

Parameter	Conventional NoC	Proposed NoC	Improvement
Power Usage	High	Low	Reduced by ~45%
Switching Activity	Continuous	On-demand	Idle switching eliminated
Latency	Standard	+1–2 cycles	Slight overhead
Suitability for IoT	Low	High	Ideal for low-duty-cycle systems

The slight increase in latency is acceptable because energy efficiency is the primary objective in IoT devices.

6.5 Result Summary

1. The proposed architecture operates only during valid events and remains idle otherwise.
2. Dual-clock FIFO enables stable synchronization between clock domains.
3. Clock-enable-based control is FPGA-safe and avoids routing/timing issues.
4. The system achieves significant energy savings with minimal performance loss.

The simulation and implementation results clearly demonstrate that the Proposed Event-Driven Dual-Domain Clock-Gated NoC is more power-efficient than the conventional synchronous NoC. The system reduces dynamic power consumption and preserves functional accuracy, making it suitable for IoT and energy-constrained embedded computing applications.

7. CONCLUSION

The proposed Dual-Domain Clock-Gated Network-on-Chip (NoC) was successfully implemented on the Xilinx Artix-7 XC7A35T FPGA, proving that ultra-low power communication can be achieved for IoT-based systems. The design operates using two separate clock domains—one for high-speed router processing and another for low-frequency peripheral and sensor nodes—allowing better performance with reduced switching activity. Clock gating is used to turn off inactive modules during idle periods, which lowers dynamic power consumption. In addition, the event-driven flit injection mechanism ensures that data is transmitted only when a valid event occurs, avoiding unnecessary communication. Hardware implementation results confirm proper multi-clock synchronization, stable operation without metastability issues, reduced power consumption compared to traditional synchronous NoC designs, efficient FPGA resource utilization, and good scalability for future IoT edge computing applications.

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