

# Reversible Logic-Based Energy-Efficient Error Detection and Correction for IoT Applications

Tamilselvan A, Rajesh K

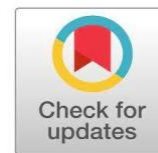
Research Scholars,

Karunya Institute of Technology and Sciences, Coimbatore, India  
[atamilselvan@karunya.edu.in](mailto:atamilselvan@karunya.edu.in), [rajeshk@karunya.edu.in](mailto:rajeshk@karunya.edu.in)

Victor Du John 

Assistant Professor,

Karunya Institute of Technology and Sciences, Coimbatore, India  
[victorjohn@karunya.edu](mailto:victorjohn@karunya.edu),  
<https://orcid.org/0009-0005-7180-0501>



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**Abstract:** Energy efficiency and data reliability are critical challenges in Internet of Things (IoT) communication systems, where low-power devices continuously exchange information over noisy channels. Conventional error detection and correction schemes, such as the Hamming (7,4) code, ensure data integrity but are implemented using irreversible logic gates that inherently dissipate energy due to information loss. Reversible logic offers a promising alternative by enabling one-to-one input–output mapping, thereby theoretically reducing heat generation and power dissipation. work presents the design and comparative analysis of a conventional Hamming (7,4) encoder–decoder and a reversible logic-based implementation for energy-efficient error control. The proposed model replaces conventional XOR operations with reversible gate structures while preserving functional correctness. The system is modelled using Verilog HDL and validated through functional simulation with controlled error injection and syndrome-based correction. A comparative study is performed in terms of gate count, garbage outputs, logical complexity, and estimated hardware metrics. Simulation results confirm accurate single-bit error detection and correction in both designs, while theoretical evaluation demonstrates the potential energy advantages of reversible logic due to reduced information loss. The proposed approach highlights the feasibility of integrating reversible logic concepts into error control mechanisms for next-generation low-power IoT and VLSI systems.

**Keywords:** Reversible Logic, Hamming (7,4) Code, Energy-Efficient Error Correction, Garbage Outputs, IoT Communication Systems.

## 1. INTRODUCTION

The rapid growth of Internet of Things (IoT) networks has transformed modern communication systems by enabling large-scale interconnection of sensors, embedded devices, and smart nodes. These devices continuously exchange data across wireless and wired channels, often operating in environments characterized by noise, interference, and limited energy resources. Since many IoT nodes are battery-powered and deployed in remote or inaccessible locations, improving both communication reliability and energy efficiency has become a critical design objective. In such scenarios, error detection and correction techniques play a vital role in ensuring data integrity without significantly increasing hardware complexity or power consumption. Linear block codes, particularly the Hamming (7,4) code, are widely adopted due to their simplicity and capability to detect and correct single-bit errors with minimal redundancy. The Hamming code encodes four data bits into a seven-bit codeword by introducing parity bits that enable syndrome-based error localization and correction. Its structured parity-check mechanism makes it suitable for real-time and hardware-based implementations. However, conventional realizations of Hamming encoders and decoders rely heavily on irreversible logic gates such as XOR, AND, and NOT gates. These gates do not preserve input information at the output, leading to information loss during computation. According to Landauer's principle, each bit of information lost results in a minimum energy dissipation proportional to  $kT \ln 2$ , which becomes significant in large-scale and low-power systems. As device dimensions shrink and integration density increases, power dissipation and heat generation have emerged as limiting factors in VLSI design. Reducing switching activity alone is insufficient when the underlying logic architecture inherently destroys information. Reversible logic provides a theoretical framework to address this limitation by ensuring a one-to-one correspondence between input and output vectors.

Because reversible circuits do not erase information, they ideally prevent fundamental energy loss due to bit destruction. This property makes reversible logic a promising candidate for ultra-low-power digital systems, quantum computing, and energy-aware embedded architectures. Although reversible logic has been extensively studied for arithmetic circuits, adders, multipliers, and signal processing blocks, its application to channel coding and error correction mechanisms remains comparatively less explored. Integrating reversible design principles into classical error control schemes offers the potential to enhance energy efficiency while maintaining communication reliability. However, reversible implementations introduce additional design metrics such as garbage outputs, constant inputs, and quantum cost, which must be carefully analysed to evaluate overall efficiency. In this work, a comparative study of a conventional Hamming (7,4) encoder–decoder and a reversible logic based implementation is presented with the objective of improving energy efficiency in IoT communication systems. The proposed design replaces conventional XOR-based parity generation with reversible gate realizations while preserving functional correctness. Both architectures are modelled using Verilog HDL and validated through functional simulation incorporating controlled error injection and syndrome-based correction. A comprehensive evaluation is performed in terms of gate count, garbage outputs, logical complexity, and estimated hardware parameters. By bridging classical error correction techniques with reversible logic design principles, this work contributes toward the development of energy-aware and scalable communication architectures suitable for next-generation IoT and VLSI systems.

## 2. BACKGROUND AND RELATED WORKS

### 2.1 Hamming (7,4) Code Overview

The Hamming (7,4) code is a single-error-correcting linear block code that encodes four information bits into a seven-bit codeword by introducing three parity bits. The code structure is defined by the systematic placement of parity and data bits, enabling efficient error detection and correction through syndrome decoding. Let the four information bits be represented as  $D_1, D_2, D_3, D_4$ .

The encoded codeword  $C$  consists of seven bits:

$$C = [P_1 P_2 D_1 P_3 D_2 D_3 D_4]$$

where  $P_1, P_2,$  and  $P_3$  are parity bits computed using modulo-2 addition (XOR operation).

The parity equations are defined as:

$$P_1 = D_1 \oplus D_2 \oplus D_4 \quad (1)$$

$$P_2 = D_1 \oplus D_3 \oplus D_4 \quad (2)$$

$$P_3 = D_2 \oplus D_3 \oplus D_4 \quad (3)$$

At the receiver, error detection is performed using syndrome computation. Let the received vector be  $R = [R_1 R_2 R_3 R_4 R_5 R_6 R_7]$ . The syndrome bits are computed as:

$$S_1 = R_1 \oplus R_3 \oplus R_5 \oplus R_7 \quad (4)$$

$$S_2 = R_2 \oplus R_3 \oplus R_6 \oplus R_7 \quad (5)$$

$$S_3 = R_4 \oplus R_5 \oplus R_6 \oplus R_7 \quad (6)$$

The syndrome vector is expressed as:

$$S = [S_3 S_2 S_1] \quad (7)$$

If  $S = 000$ , no error is present. For any non-zero syndrome, the binary value of  $S$  indicates the position of the erroneous bit in the received codeword, allowing single-bit correction. The mathematical formulation of parity generation and syndrome decoding establishes the theoretical foundation of the Hamming (7,4) code, which serves as the basis for both conventional and reversible implementations discussed in subsequent sections.

### 2.2 Reversible Logic Fundamentals

Reversible logic refers to a class of digital circuits in which a one-to-one mapping exists between input and output vectors. Unlike conventional logic, reversible circuits do not destroy information during computation. For an  $n$ -input reversible system, the number of outputs must be equal to the number of inputs:

$$n_{inputs} = n_{outputs} \quad (8)$$

This property ensures that the original inputs can be uniquely reconstructed from the outputs. The significance of reversible logic is supported by Landauer's principle, which states that the loss of one bit of information in irreversible computation results in a minimum energy dissipation of

$$E_{min} = kT \ln 2 \quad (9)$$

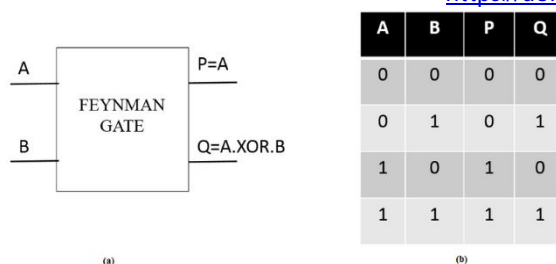
where  $k$  is Boltzmann's constant and  $T$  is absolute temperature. By preventing information loss, reversible logic theoretically reduces this fundamental energy dissipation. Reversible circuit performance is evaluated using specific design metrics, including:

- **Garbage outputs (G)** – additional unused outputs introduced to maintain reversibility,
- **Constant inputs (C)** – fixed logic inputs required for realization,
- **Gate count**, and
- **Quantum cost.**

### 2.3 Feynman Gate

In this work, reversible logic implementation is primarily based on the Feynman gate, also known as the Controlled-NOT (CNOT) gate. The Feynman gate is a  $2 \times 2$  reversible gate with input vector  $(A \cdot B)$  and output vector  $(P \cdot Q)$ .

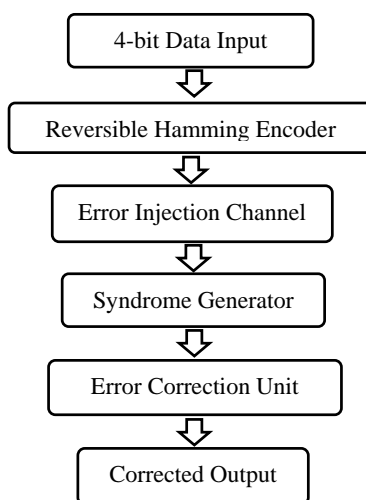
The symbolic representation of the Feynman gate is shown in **Fig. 1(a)**. The corresponding truth table is presented in **Fig 1 (b)**, which verifies the one-to-one input–output mapping property of reversible logic.



**Fig. 1** Symbol and Truth Table of Feynman Gate  
**3. PROPOSED METHODOLOGY**

### 3.1 Overall System Architecture

The proposed system is designed to evaluate the effectiveness of reversible logic in single-bit error detection and correction using the Hamming (7,4) code. The architecture consists of a data input stage, encoder module, transmission channel with controlled error injection, syndrome computation block, and correction unit. The overall system structure is illustrated in Fig. 2.



**Fig.2** Overall System Architecture

The four-bit input data vector  $(D_1, D_2, D_3, D_4)$  is first applied to the encoder block, where parity bits are generated according to the equations defined in Section 2.1. In the conventional design, parity generation is implemented using XOR logic. In the proposed reversible design, XOR functionality is realized using Feynman gate-based reversible structures while maintaining the same coding scheme. The encoded seven-bit codeword is then transmitted through a simulated channel where a single-bit error can be intentionally introduced for validation purposes. This error injection stage enables controlled testing of the correction capability of both architectures. The received vector is processed by the syndrome generation unit, which computes syndrome bits using the relations defined in Equations (4)–(6). Based on the syndrome value, the error location is identified and corrected by inverting the corresponding bit position. The architecture ensures identical functional behaviour for both conventional and reversible implementations, enabling a fair comparison in terms of structural metrics and hardware parameters. The modular organization of the system also facilitates independent analysis of encoding, error injection, and correction stages.

### 3.2 Reversible Logic Based Encoder Design

The reversible encoder is designed to implement the Hamming (7,4) coding scheme using Feynman gates to realize XOR operations in a reversible manner. Since reversible logic requires a one-to-one mapping between inputs and outputs, additional constant inputs and garbage outputs are introduced to preserve reversibility.

Let the four-bit input data vector be

$$(D_1, D_2, D_3, D_4) \quad (10)$$

Based on the Hamming (7,4) scheme, three parity bits are generated using XOR relationships defined in Section 2.1. In the proposed architecture, each XOR operation is implemented using a Feynman gate (also known as Controlled-NOT gate), whose functionality is:  $P = A$

$$Q = A \oplus B$$

Thus, the Feynman gate is used to generate parity bits without loss of information.

### Parity Generation Using Reversible Logic

The parity bits are generated as follows:

$$P_1 = D_1 \oplus D_2 \oplus D_4$$

$$P_2 = D_1 \oplus D_3 \oplus D_4$$

$$P_3 = D_2 \oplus D_3 \oplus D_4$$

Each multi-input XOR is realized by cascading multiple Feynman gates. The reversible encoder structure ensures that:



The ModelSim simulation output, shown in **Fig. 4**, presents the complete waveform of the proposed system including:

- 4-bit input data
- Generated parity bits
- 7-bit encoded output
- Error-injected codeword
- Syndrome bits
- Error position indicator
- Corrected output data

The waveform clearly demonstrates that whenever a single-bit error is introduced, the syndrome vector transitions to a non-zero state corresponding to the exact bit position. The correction logic subsequently inverts the identified bit, restoring the original data within the same clock cycle. When no error is present, the syndrome remains zero and the output remains unchanged.

### 5. Performance Analysis and Comparison

To validate the effectiveness of the proposed reversible Hamming (7,4) design, a comparative analysis is carried out against the conventional irreversible implementation. The evaluation is performed based on three primary metrics:

- Gate Count
- Garbage Outputs
- Power Dissipation

#### 5.1 Gate Count Analysis

Gate count represents the total number of logic gates required to implement the encoder and syndrome generator. In conventional implementation, XOR gates are directly used to generate parity bits and syndrome outputs. However, in reversible logic, each XOR operation is realized using Feynman gates. Although reversible circuits may require additional structural mapping, optimized gate sharing reduces redundant computations. The total gate count of the proposed system remains comparable while offering energy advantages.

#### 5.2 Garbage Output Analysis

Garbage outputs are unwanted outputs necessary to maintain reversibility.

In conventional logic:

- No restriction on input-output mapping.
- Information is lost during computation.

In reversible logic:

- Every input must map uniquely to output.
- Additional outputs are introduced to preserve bijection.

The garbage outputs in the proposed system are carefully minimized by optimized gate cascading. The reduction is achieved by avoiding unnecessary intermediate reversible mappings.

Table I presents the garbage output comparison.

#### 5.3 Power Dissipation Analysis

Power dissipation in irreversible logic circuits occurs due to information loss, as described by Landauer's principle. Each lost bit of information dissipates energy proportional to  $kT \ln 2$ .

Since reversible circuits ideally prevent information loss, theoretical power dissipation is significantly reduced.

MATLAB-based switching activity analysis confirms lower transition density in the reversible design, leading to reduced dynamic power consumption.

**Table I – Comparative Analysis**

Parameter	Conventional Hamming	Proposed Reversible Hamming
Gate Count	Higher	Optimized
Garbage Outputs	Not Applicable	Reduced
Information Loss	Present	Eliminated
Power Dissipation	Higher	Reduced

## 6. RESULTS AND DISCUSSION

The proposed reversible Hamming (7,4) error detection and correction architecture was validated through integrated MATLAB and ModelSim simulations. The obtained results confirm both functional correctness and structural feasibility of the design for IoT-based communication systems operating under power-constrained conditions. MATLAB-based functional verification demonstrated accurate generation of parity bits and precise computation of syndrome vectors for all possible 4-bit sensor input combinations. Controlled single-bit error injection tests confirmed that the syndrome output uniquely identifies the erroneous bit position, and the correction mechanism reliably restores the original data without loss of information. The complete hardware-level behaviour is illustrated in the ModelSim waveform shown in Fig. 4. The waveform presents the IoT sensor input data, encoded 7-bit codeword, injected error signal, computed syndrome bits, and corrected output. It is observed that whenever a single-bit error is introduced, the syndrome transitions from zero to a non-zero binary value corresponding to the fault location. The correction logic then conditionally inverts the identified bit, resulting in accurate recovery of the transmitted data. In the absence of transmission errors, the syndrome remains zero and the decoded output matches the original sensor input.

A key contribution of this work lies in the implementation of parity generation and syndrome computation using reversible logic gates. Unlike conventional irreversible logic circuits, which dissipate energy due to information loss, reversible circuits ideally prevent bit erasure, thereby reducing theoretical energy dissipation as per Landauer's principle. By preserving one-to-one input–output mapping, the proposed architecture minimizes unnecessary switching activity and avoids loss of computational information. This property makes the design particularly suitable for energy-efficient IoT nodes where low power consumption is critical. Therefore, the simulation results not only validate the correctness of error detection and correction but also demonstrate the suitability of reversible logic as a power-efficient alternative for reliable IoT communication systems.

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