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An Efficient Nonlinear Control of the Seven-Level PUC Rectifier

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Abstract— A novel nonlinear control of the seven level packed U cells (PUC) converter is proposed in this paper. The proposed control technique is based on the converter averaged modelling. It was designed to draw a sinusoidal line current with a unity power factor operation. Since harmonics contents of line current and rectifier input voltage are very low thereby active and passive filters ratings are highly reduced resulting on a very high energetic efficiency and a reduced installation cost. The proposed concept was verified by simulation performed in Matlab Simulink environment. The experimental validation was carried out through implementation using dSpace DS1103 environment.

Keywords— PUC, multilevel converters, active rectifier, averaged modelling, nonlinear control, harmonic reduction

I. INTRODUCTION

Multilevel converters are, nowadays, widely used in several applications like high-voltage high-power domain, electrical drives, renewable energy systems, active filtering, telecommunication etc. Among these converters, PUC topology [1-6] has proven its competitiveness. In fact, traditional multilevel converters like neutral point clamped converters NPC, proposed by Nabae, Takahashi and Akagi [7], and Flying Capacitors Converters FCC, proposed by Meynard and Foch [8], and Cascaded H-Bridge CHB topology [9-11] present many drawbacks if the number of voltage levels grows which results on high cost and a bulky installation. When the number of desired voltage level exceeds three, becomes the optimal solution. The CHB topology requires independent and isolated DC voltage sources, which leads to the use of transformers.

Both sinusoidal pulse width modulation PWM [1-3] and hysteresis current techniques [4-6] have been used to control the PUC converters. The second strategy has very simple implementation but it presents a sporadic switching frequency, whereas the first strategy has a complex implementation but is characterized by a constant switching frequency. The hysteresis control technique has proven to be suitable solution for all the applications of current controlled voltage source inverters where performance requirements are more demanding, such as active filters, drives and high-performance ac power conditioners, albeit at the expense of variable switching frequency. In this paper, a nonlinear control strategy is proposed. An averaged model of the seven-level PUC rectifier is designed to allow high dynamic performances of source-converter-load system even in case of severe load change. In fact, the DC-link and auxiliary DC-bus voltages remain well regulated even during transient mode. The line current is nearly sinusoidal which permit to avoid passive filters resulting on a very high energetic efficiency and a reduced installation cost.

II. PRESENTATION OF THE SEVEN-LEVEL PUC RECTIFIER

The 7-level PUC converter uses only six switches and two capacitors whereas the 7-level NPC and FCC converters use twelve switches and six capacitors. The CHB converter, however, uses twelve switches and three capacitors. Since each leg of the 7-level PUC rectifier makes use of three power switches (T1, T2 and T3 or T'1, T'2 and T'3), then there is eight possible states which are depicted in fig.1. Noticing that states 4 and 5 are redundant, then the rectifier input voltage is constituted only from seven voltage levels. Knowing that the voltage V2 is controlled to be the third of V1, so these levels are (V1, 2V1/3, V1/3, 0, -V1/3, -2V1/3, -V1).

Fig. 2 shows the holding voltage of T1, T2, and T3 switches for a seven-level converter with V 1 = 150 V and V 2 = 50 V, operating under sinusoidal modulation. The rectifier input voltage V_{AN} is the sum of switches voltages as depicted by the experimental results shown in fig.2. The seven levels are (150V, 100V, 50V, 0, -50V, -100V, -150V).

While observing the behaviour of voltages V_{T1}, V_{T2}, and V_{T3}, one can notice the potential of using a combination of two types of semiconductor devices technologies (GTO and IGBT) in high power conversion scheme. In fact, the major drawback of the GTO technology is its limited switching frequency; whereas, IGBT technology cannot sustain high power, while operating at medium frequency. The combination of two GTOs and four IGBTs in the seven-level PUC topology permits to achieve optimally designed and efficient high power conversion unit.

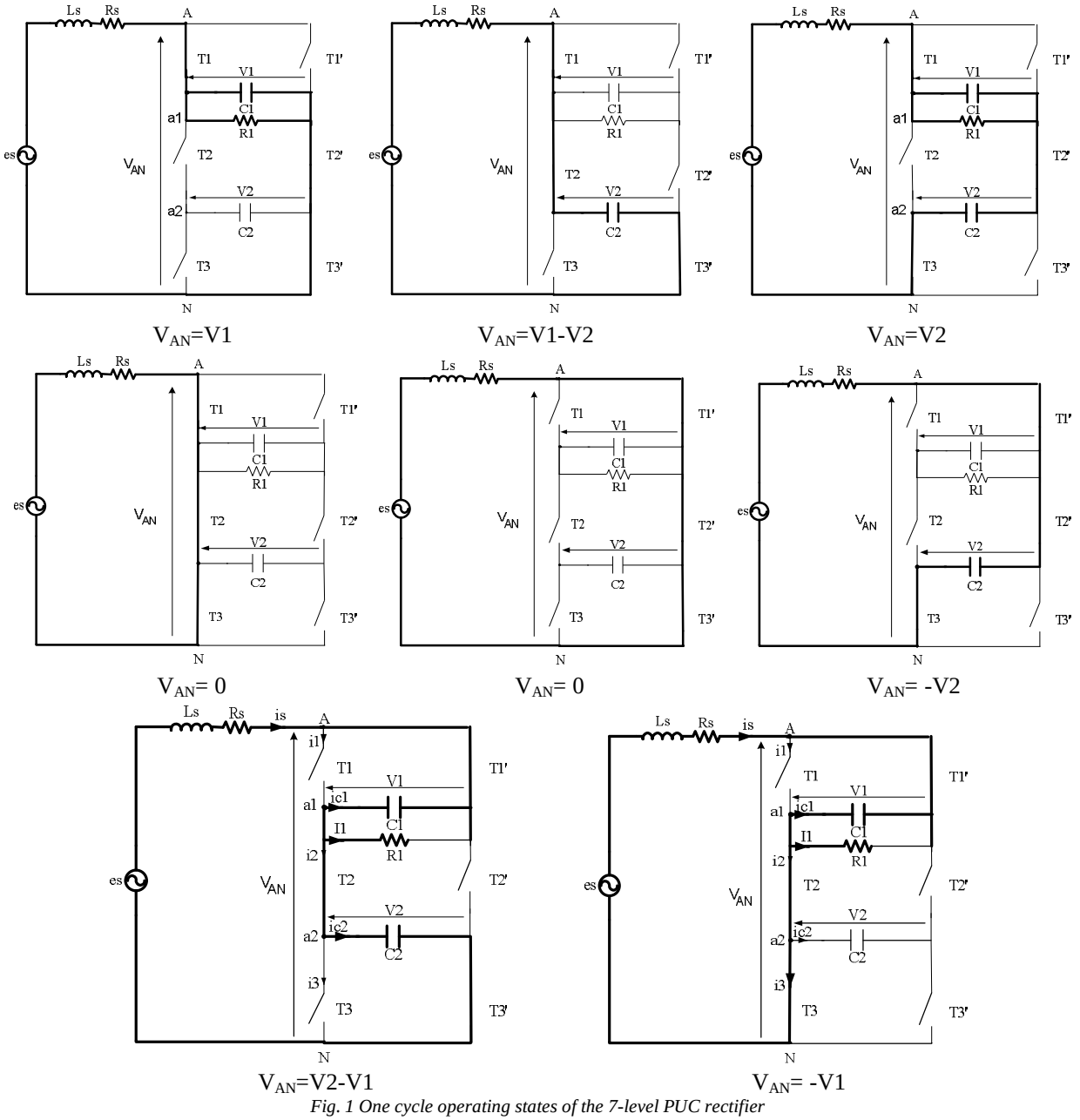


Fig. 1 One cycle operating states of the 7-level PUC rectifier

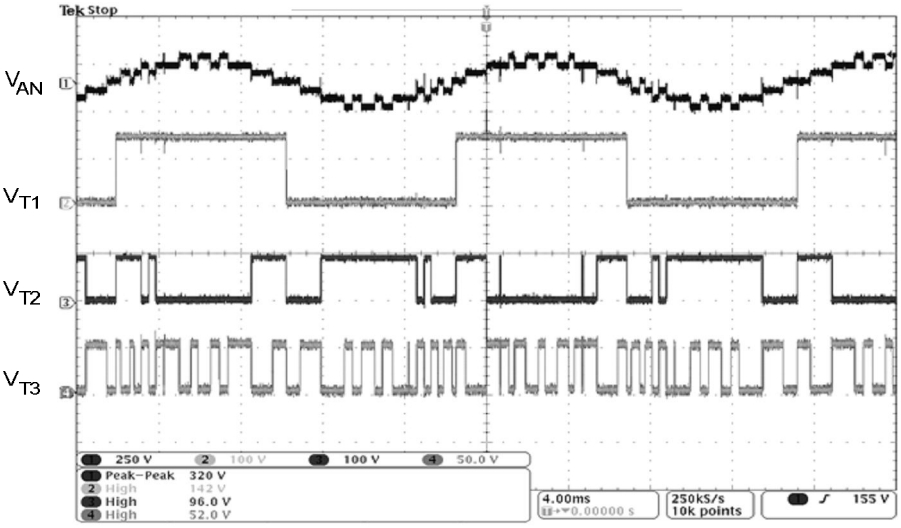


Fig. 2 Rectifier input voltage and holding voltage of different T_i switches

III. THE PROPOSED NONLINEAR CONTROL OF THE 7-LEVEL PUC RECTIFIER

All T_i and T_i' switches (fig.1) operate complementarily. Let S_i be a switching function of T_i switch where i={1, 2, 3}. S_i is defined by:

$$S_i = \begin{cases} 1 \text{ if } T_i \text{ is ON} \\ 0 \text{ if } T_i \text{ is OFF} \end{cases} \quad (1)$$

From fig. 1, we can write:

$$\begin{cases} V_{Aa1} = -S1.V1 \\ V_{a1a2} = S2(V1 - V2) \\ V_{a2N} = S3.V2 \end{cases} \quad (2)$$

We can write also:

$$\begin{cases} i1 = S1.is \\ i2 = S2.is \\ i3 = S3.is \end{cases} \quad (3)$$

Adding V_{Aa1}, V_{a1a2} and V_{a2N} gives:

$$V_{AN} = V_{Aa1} + V_{a1a2} + V_{a2N} = (S2 - S1).V1 + (S3 - S2).V2 \quad (4)$$

Applying Kirchhoff's Current Law (KCL) to the node a1 gives:

$$i1 = i2 + ic1 + I_1 \quad (5)$$

ic1 et I1 are the C1 capacitor current and the C1 capacitor load current respectively.

$$ic1 = C1.\frac{dV1}{dt} = i1 - i2 - I_1 \quad (6)$$

Thus, we can write:

$$\frac{dV1}{dt} = \frac{(S1 - S2).is}{C1} - \frac{I_1}{C1} \quad (7)$$

By the same, applying Kirchhoff's Current Law (KCL) to the node a2 gives:

$$i2 = i3 + ic2 + I_2 \quad (8)$$

So we can conclude:

$$\frac{dV2}{dt} = \frac{(S2 - S3).is}{C2} \quad (9)$$

Applying Kirchhoff's Voltage Law to the converter input loop gives:

$$V_{AN} = -R_s.is - L_s\frac{dis}{dt} + e_s \quad (10)$$

By comparing (4) and (10), we can conclude:

$$\frac{dis}{dt} = \frac{e_s - R_s.is - (S2 - S1).V1 - (S3 - S2).V2}{L_s} \quad (11)$$

Let d1, d2 and d3 be duty cycles of switches T1, T2 and T3 respectively. Duty cycles are defined by:

$d1 = \frac{1}{Ts}\int_0^{Ts} S1dt$, $d2 = \frac{1}{Ts}\int_0^{Ts} S2dt$ and $d3 = \frac{1}{Ts}\int_0^{Ts} S3dt$ where Ts is the switching period.

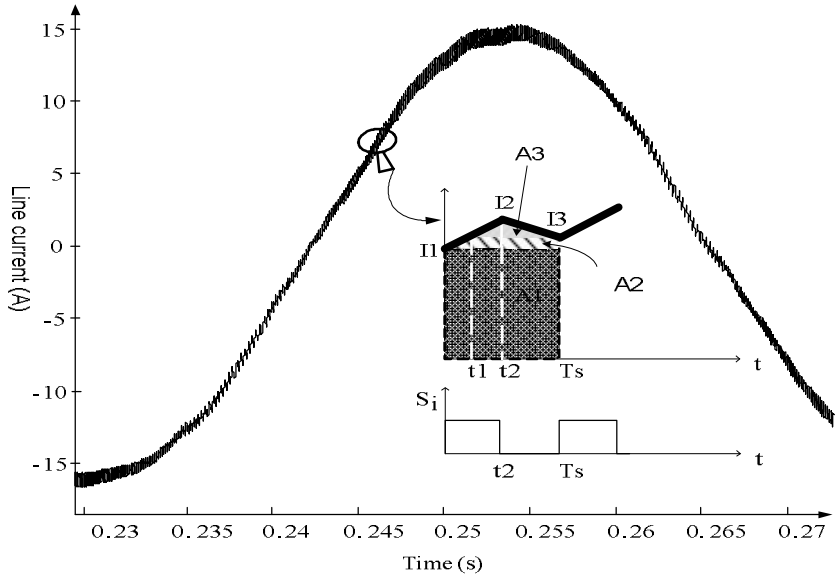


Fig. 3 PWM current waveform

According to fig.3, the duty cycle can be given by: $d_i = \frac{t2}{Ts}$

If t2=Ts, then S_i is equal to 1 all over the modulating period Ts, However, if t2=0, then S_i is null. In these cases the duty cycle is equal to the switching period (d_i=S_i). In general, they are different ($d_i = \frac{t2}{Ts} \neq S_i$).

Considering fig.3, the mean value of line current during one modulating period can be given by:

$$\bar{I} = \frac{1}{T_s}\int_0^{Ts} is.dt = \frac{1}{T_s}(T_s.I_1) + \frac{1}{T_s}\left((T_s - t1).\frac{I_2 - I_3}{2}\right) + \frac{1}{T_s}\left(t1.\frac{I_3 - I_1}{2} + (T_s - t1).(I_3 - I_1)\right) \quad (12)$$

The three areas A1, A2 and A3 on fig.3 can be written as: $A_1 = T_s.I_1$ (dark gray area), $A_2 = (T_s - t1).\frac{I_2 - I_3}{2}$ (light gray area) and $A_3 = t1.\frac{I_3 - I_1}{2} + (T_s - t1).(I_3 - I_1)$ (shaded area).

Considering the assumption that A_1>>(A_2+A_3), which is justified by the low ripple of current. This leads to consider that the line current remains constant in a modulating period. One can conclude that:

$$\frac{1}{T_s}\int_0^{T_s} S_i.i_s.dt = \frac{i_s}{T_s}\int_0^{T_s} S_i.dt = i_s.d_i \quad (13)$$

Let x_1, x_2 and x_3 be the state variables of the source-converter-load system defined by:

$$x_1 = i_s, \; x_2 = V1 \text{ and } x_3 = V2$$

Then, the system state equation is given by:

$$\begin{cases} \frac{dx_1}{dt} = \frac{e_s - R_s.x_1 - (d2 - d1).x_2 - (d3 - d2).x_3}{L_s} \\ \frac{dx_2}{dt} = \frac{(d1 - d2).x_1}{C1} - \frac{I_1}{C1} \\ \frac{dx_3}{dt} = \frac{(d2 - d3).x_1}{C2} \end{cases} \quad (14)$$

Thereby, the proposed average model of the 7-level PUC rectifier is shown in fig.4.

By considering the duty cycles as inputs: u1=d1, u2=d2 and u3=d3, the model of the source-converter-load system can be written as the following matrix equation:

$$\frac{dX}{dt} = F(X) + G(X).U + C \tag{15}$$

Where: $X = \begin{bmatrix} x1 \\ x2 \\ x3 \end{bmatrix}$, $F(X) = \begin{bmatrix} \frac{-R_s x_1}{L_s} \\ 0 \\ 0 \end{bmatrix}$, $C = \begin{bmatrix} \frac{e_s}{L_s} \\ \frac{-I_1}{C1} \\ \frac{-I_2}{C2} \end{bmatrix}$, $U = \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix}$ and $G(X) = \begin{bmatrix} \frac{x_2}{L_s} & \frac{x_3 - x_2}{L_s} & \frac{-x_3}{L_s} \\ \frac{x_1}{C1} & \frac{-x_1}{C1} & 0 \\ 0 & \frac{x_1}{C2} & \frac{-x_1}{C2} \end{bmatrix}$

The determinant of matrix G is null, then G is not invertible. Noting that state variables x2 and x3 serve to generate x1 reference, then we can exclude one of them. The problem is solved using the following assumption: $u_1 + u_2 + u_3 = 1.5$. Inputs u_1, u_2 and u_3 vary between 0 and 1, so one can choose to center them in their variation intervals. Applying a PI linear control method to each subsystem gives:

$$u_{11} = -\left(x_{1ref} - x_1\right)\left(K_{p11} + \frac{K_{i11}}{s}\right),\ u_{21} = -\left(x_{2ref} - x_2\right)\left(K_{p21} + \frac{K_{i21}}{s}\right) \text{ and } u_{31} = -\left(x_{3ref} - x_3\right)\left(K_{p31} + \frac{K_{i31}}{s}\right)$$

The reference of the variable x2 is the desired DC link voltage, whereas, x3 reference is its third. The reference of the state variable x1 is the sum of u_{11}, u_{21} and u_{31}. Finally, the input vector is given by:

$$\begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} = \begin{bmatrix} \frac{x_2 + x_3}{3x_1x_3} & \frac{-1}{3x_2} & \frac{1}{3} \\ \frac{x - 2x_3}{3x_1x_2} & \frac{2}{3x_2} & \frac{1}{3} \\ \frac{-2x_2 - x_3}{3x_1x_2} & \frac{-1}{3x_2} & \frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} u_{11} + \frac{R_s x_1 - e_s}{Ls} \\ u_{31} \\ 1.5 \end{bmatrix} \tag{16}$$

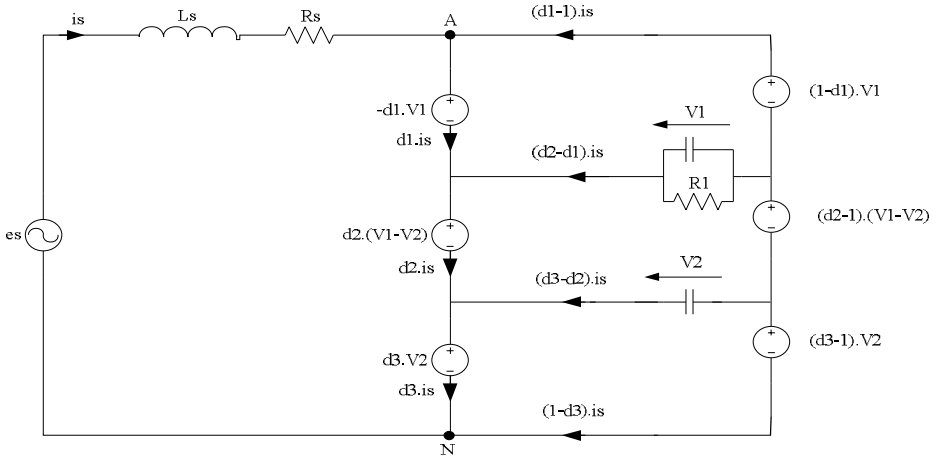


Fig. 4 The proposed average model of the 7-level PUC rectifier

The synoptic scheme of the proposed nonlinear control technique is illustrated in fig.5.

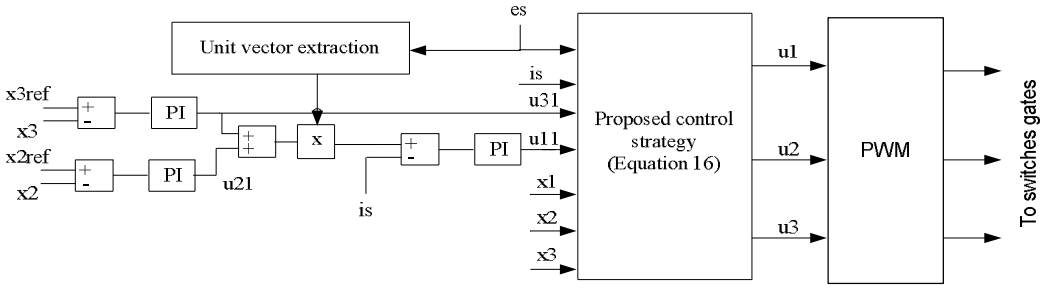


Fig. 5 The proposed nonlinear control strategy

IV. SIMULATION RESULTS

The system parameters are as follows, line inductance, line resistance, load resistance, capacitors values are equal to 3mH, 0.1Ω, 40Ω and 4000μF respectively. The auxiliary DC bus voltage must be regulated to the third of the DC-link voltage which is controlled to 100V. The root mean square RMS voltage of the supply network is fixed to 50V.

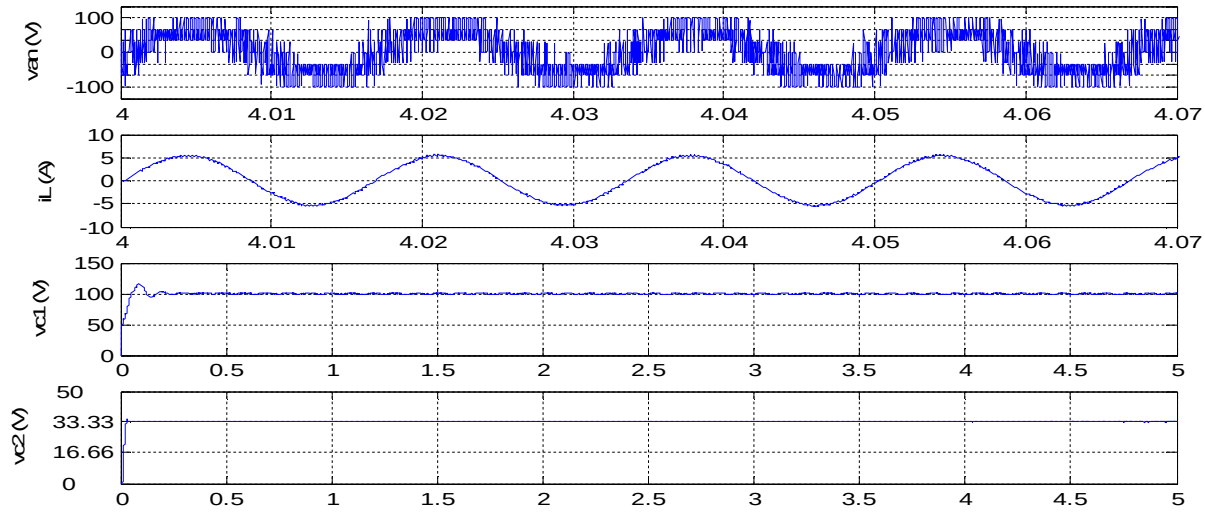


Fig. 6 Evolution of the rectifier input voltage V_{AN}, line current i_L, DC-link and auxiliary DC bus voltages

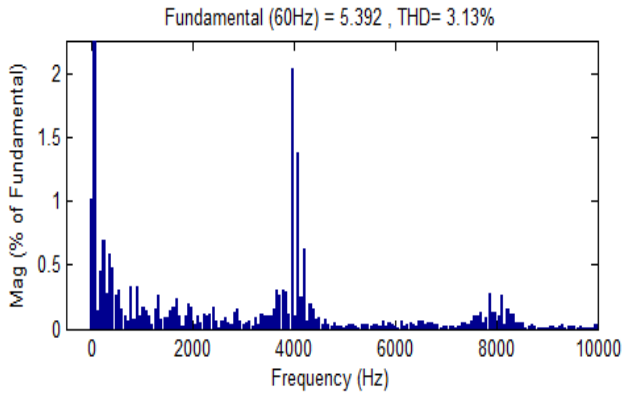


Fig.7 Harmonics spectrum of line current

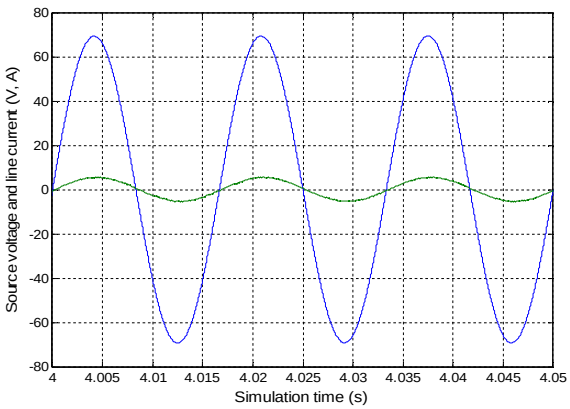


Fig. 8 Source voltage and line current waveforms

Fig.6 shows that DC-link voltage is well controlled to its reference which is 100V, however, the auxiliary DC bus remains around the third of this value. In this figure, one can notice that the rectifier input voltage is constituted from seven levels which are (100V, 66.66V, 33.33V, 0, -33.33V, -66.66V, -100V). Load current is perfectly sinusoidal as shown in the same figure. Its total harmonics distortion THD is about 3% which is very small without use of any filters (see fig.6). The proposed control strategy insures a unity power factor operation as depicted by fig.7.

V. EXPERIMENTAL RESULTS

Three Analog to Digital converters (ADC) of the dSpace DS1103 are used to acquire load current i_L, principal and auxiliary DC-bus voltages respectively V1 and V2. An electronic circuit is designed for sensing these signals. Six digital I/O are used to output the MOSFET gate pulses. An opto-isolated interface board is also designed to isolate the low power logic signals from the power stage. The PolarHV^{TM}, HiPerFET, IXF44N50P MOSFET devices were chosen as power switches. The power stage parameters were chosen like those chosen for simulation. The supply voltage is fixed at the RMS value of 50V. Both principal and auxiliary DC buses voltages are regulated to be equal to 100V and 33.33V respectively. Due to the PCB limitations, the minimum load resistance was chosen to have a peak value below 6A. The DC buses are well regulated as shown by fig.9 and fig.10. Line current is nearly sinusoidal and attains a peak value of 5.4A (RMS value is 3.83A).

By comparing experimental and simulation results, one can conclude the high concordance of these results. In order to prove the high dynamics of the proposed control technique, a severe load change is considered. Indeed a load step from 40Ω to 80Ω and inversely is imposed. A loop effect on the system response after the change from 80 to 40 is shown in fig.11.a, whereas fig 11.b depicts a zoom on transient during the inverse step. One can notice the good response of the whole system.

VI. CONCLUSION

An efficient nonlinear control technique for the seven level packed U cells converter was presented in this paper. The DC link buses voltages are well controlled and track their references even under 100% of load steps. The proposed controller allows a nearly sinusoidal supply network current and a rectifier input voltage with seven levels. The low total harmonics distortion, THD, of line current permits to avoid or even to reduce the rating of active and passive filters resulting on a very high energetic efficiency and a reduced installation cost. The unity power factor operation was well maintained even during transient. The response to ±100% load variations shows good dynamics behaviour of the source-converter-load system which proves the efficiency of the proposed controller.

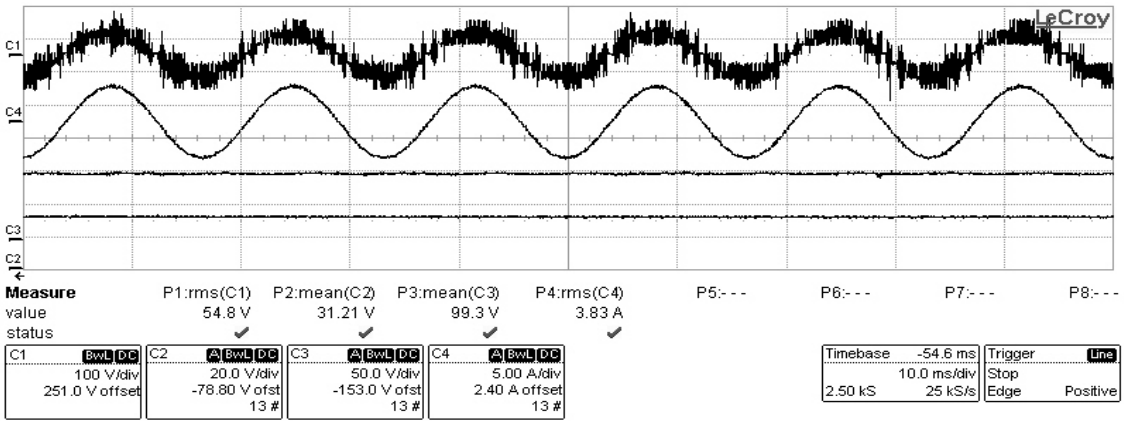


Figure 9: Experimental waveforms showing rectifier input voltage, supply current and DC bus voltages

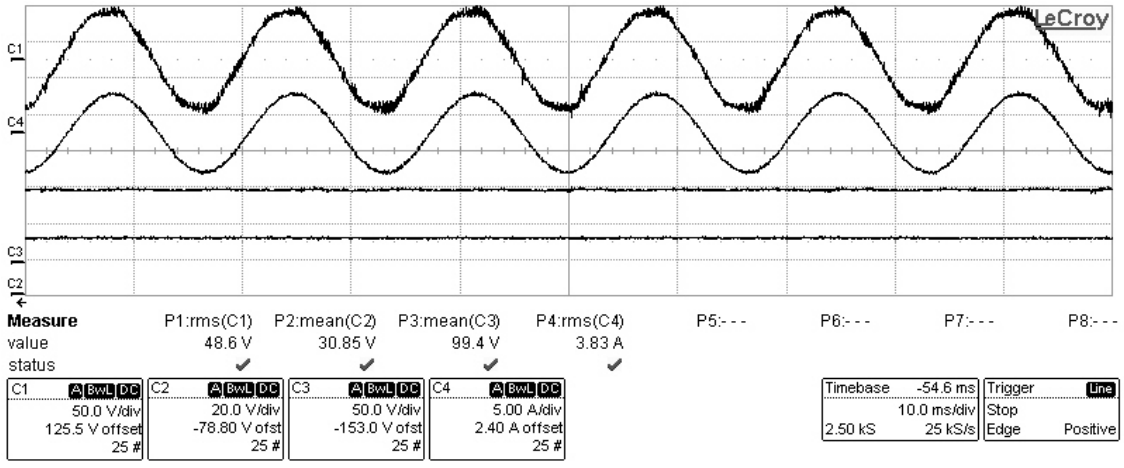
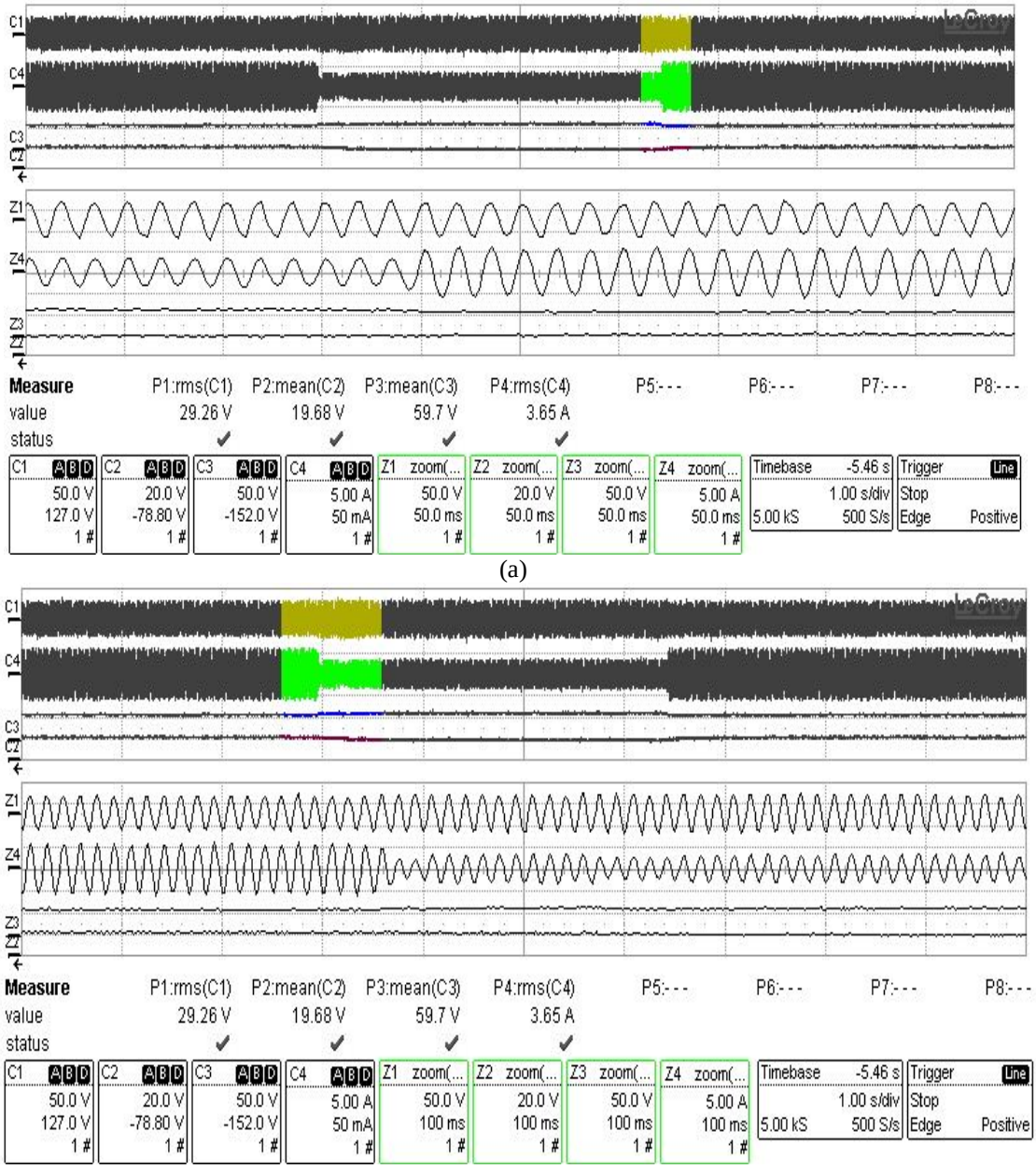


Figure 10: Experimental waveforms showing Supply voltage, supply current and DC bus voltages



(a)

(b)

Figure 11: Experimental waveforms showing Supply voltage, supply current and DC bus voltages during load change with loop effect

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